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Test for 2nd level trigger ("Accept" and "Reject")

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for J-PARC E15/E17 collaboration

0. Scheme

0. We consider to make a coincidence of two trigger signals A, B. (Then, we assume B comes later, and ***not in time for gates***).

1. Gate signals for all detectors (chambers, counters, semi-conductor detectors･･･) are produced by first level trigger A.

2. Second level triggers:

＊A∩B –> start signal of acquisition of data followed by all module clear (box initialization).

Large dead time (≡T_A, 100~1000 μsec. T_A=700 μsec for the next calc.).

＊A∩Bbar –> start signal of all module clear.

Small dead time (≡T_C, 1~10 μsec. T_C = 10 μsec for the next calc.).

1. Scientific Merit

Case-by-case dead time estimations for E17 condition.

A: K × CDH :1.5 kevents/sec B: SDD (***not the single rate***. The hit number in the timing gate defined by A): 10 events/sec

$R_{DAQ}(i)$: $(T-T_D(i))/T$, T is the spill duration, 0.7sec, $T_D(i)$ is the dead time for case i.

＊ Case 0 (First level trigger A∩B is used exclusively to acquire. B is in time as gates : KEK-E471/E549 case. **Not realistic**, but just for comparison・・・.) :

$T_D(0) = R_{DAQ}(0) \times N(A \cap B) \times T_A$ -> **$R_{DAQ}(0) = 99.3\%$**

＊ Case 1 (First level trigger A is used exclusively to acquire. B is not required hardware-wise : KEK-E570 case) :

$T_D(1) = R_{DAQ}(1) \times N(A) \times T_A$ -> **$R_{DAQ}(1) = 48.8\%$**

＊ Case 2 (First level trigger A and the second levels A∩B / A∩Bbar is separately adopted : J-PARC E17) :

$T_D(2) = R_{DAQ}(2) \times N(A \cap \mathrm{Bbar}) \times T_C + R_{DAQ}(2) \times N(A \cap B) \times T_A$ -> **$R_{DAQ}(2) = 97.8\%$**

=> **Dead time is drastically reduced compared to the case that A is simply all acquired by the first level.**

2. System Ingredients and Construction

M. Shiozawa et al, IEEE Conference Record Vol. 2 issue 30, 632-635 (1994)

- PC-VME interface : Bit3-620
- VME-TKO interface : SMP (VME side) and SCH (TKO side)
- VME modules : SMP / V002(Indicator) / RPV-100(Scaler)
- TKO modules : SCH / T002(Indicator) / RPT-140(HR TDC) /RPT-040(DC TDC) / T004(QDC) / T005(PH ADC)
- software : vmehb(vmedrv) : device driver
  vmelib-1.4 : access to VMEbus
  UNIDAQ : DAQ software

  => with no specific modification of any codes
- Hardware Trigger : normal NIM system.

All ingredients are identical to the present system. ***Only trigger construction and VETO scheme should be carefully considered***.

SMP functionality

3. Execution of the Sparse Data Scan (SDS) sequence

(i) set the value “1” to a specific bit of CMR (CoMmand Register)

(ii) ACCEPT signal input ← **Presently adopted, and kept this time as well.**

7. Initialization (issue F(15) to all M,S) of TKO Box

(i) set the value “1” to a specific bit of CMR

(ii) ACCEPT signal input

(iii) REJECT signal input ← **This time activated *additionally*.**

For (i) and (ii) of the both, PSEL[0:4] bits of STAR (STAtus Register) must be set properly in advance.

＊ A ∩ B –> ACCEPT

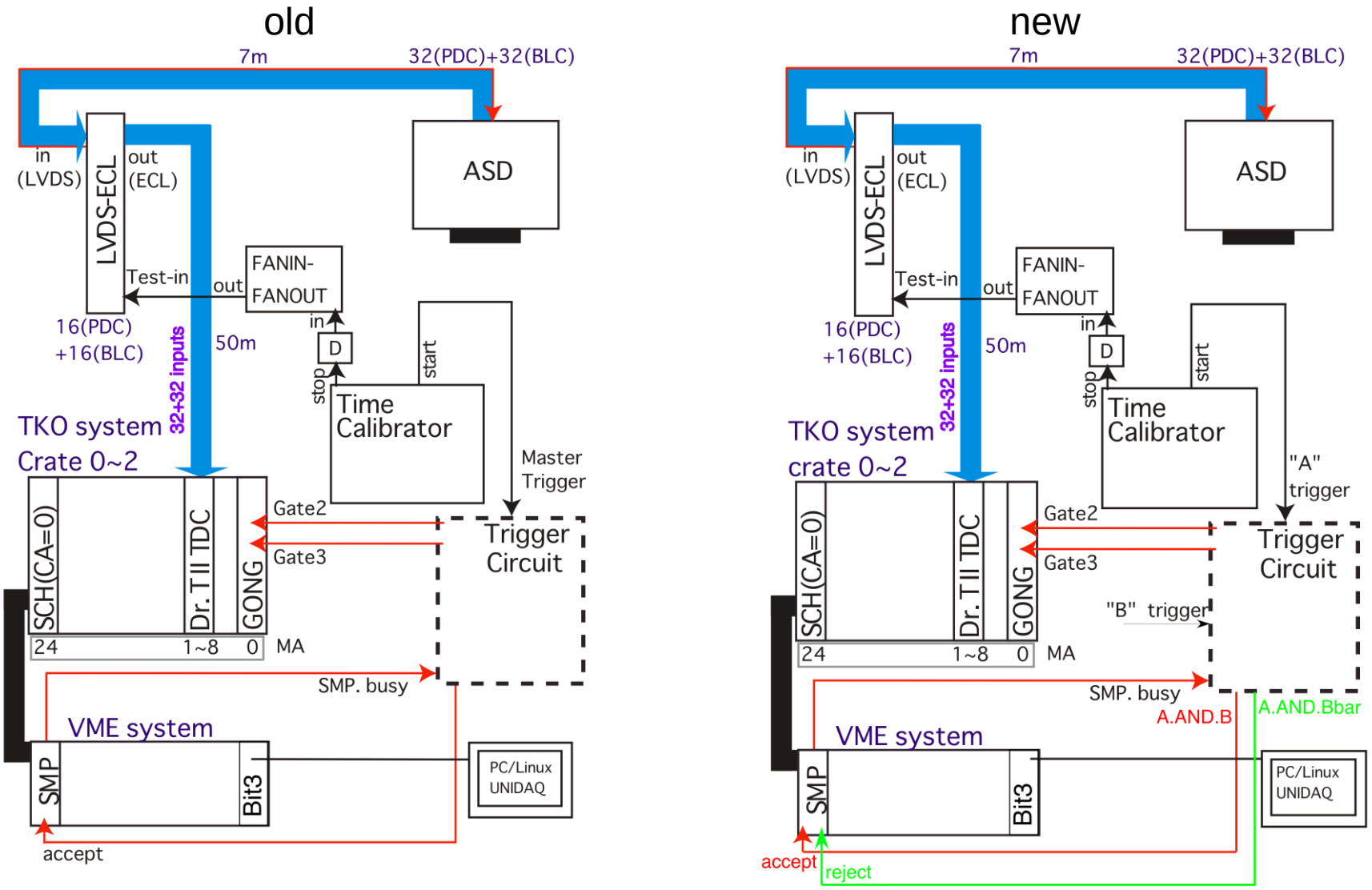
＊ A ∩ Bbar –> REJECT

e.g. A: K ×CDH / “beam” | B: SDD –> E17 E30 –> no 2nd level.

A: K ×CDH | B: NC / Pstop –> E15 / E28 / E31

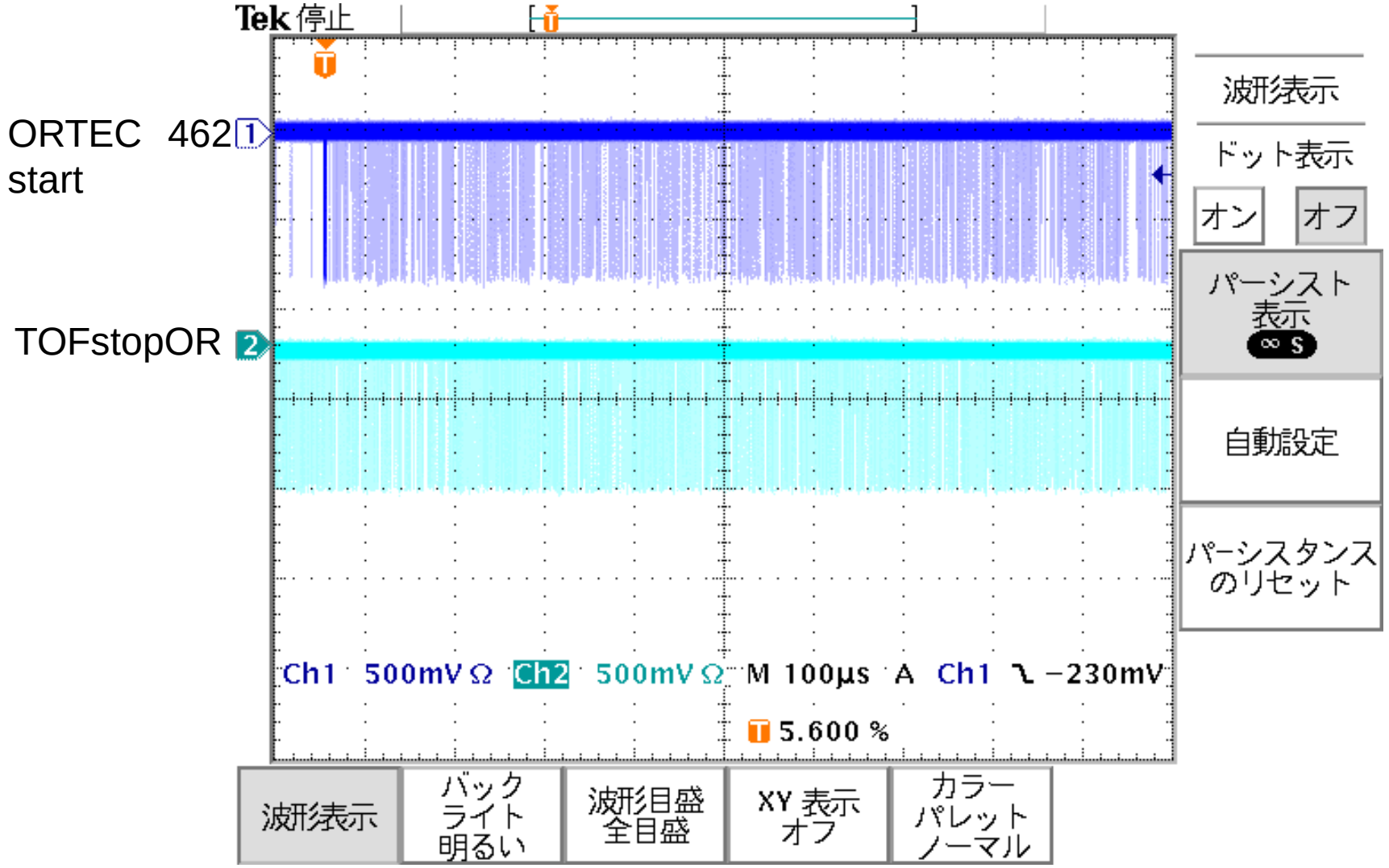
A: p / K / π / e | B:TOFstop –> K1.8BR TOF measurement

Comparison of new and old systems



They are very similar. **Construction of the "Trigger Circuit" is a key issue**.
This time TOFstopOR(~3.3 kHz) is adopted as "B" trigger optionally selected.

Time structures of Trigger Signals

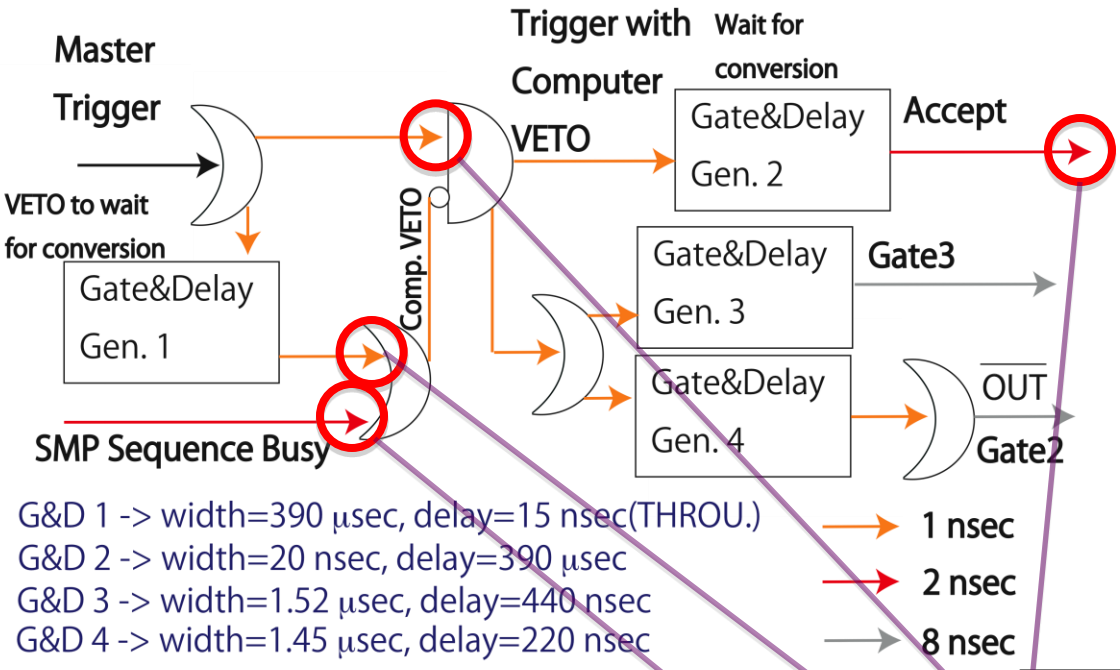


✔ No timing correlation between time calibrator start signals.

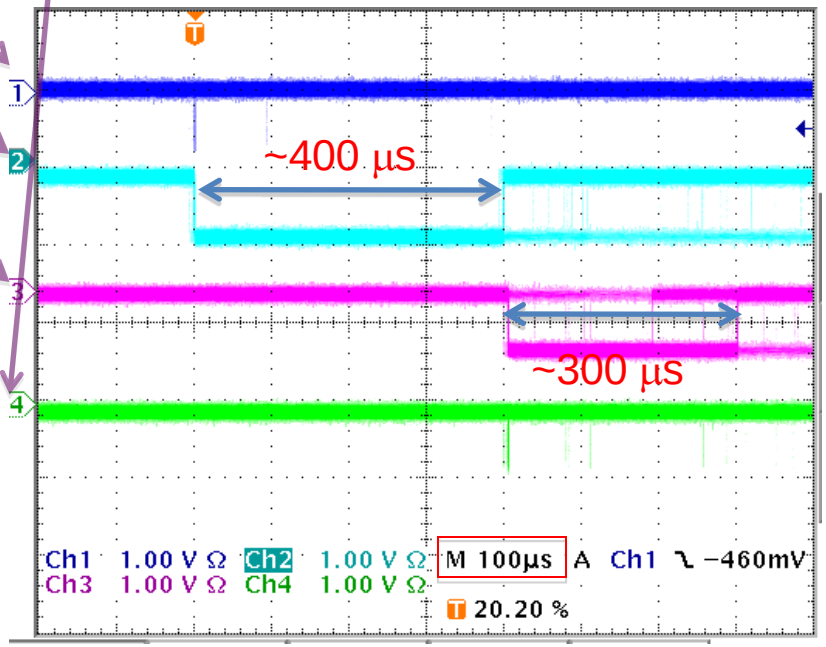
 No timing correlation between time calibrator start and TOFstopOR.

=>**They suit well for the test.**

Present Trigger Circuit/VETO Scheme



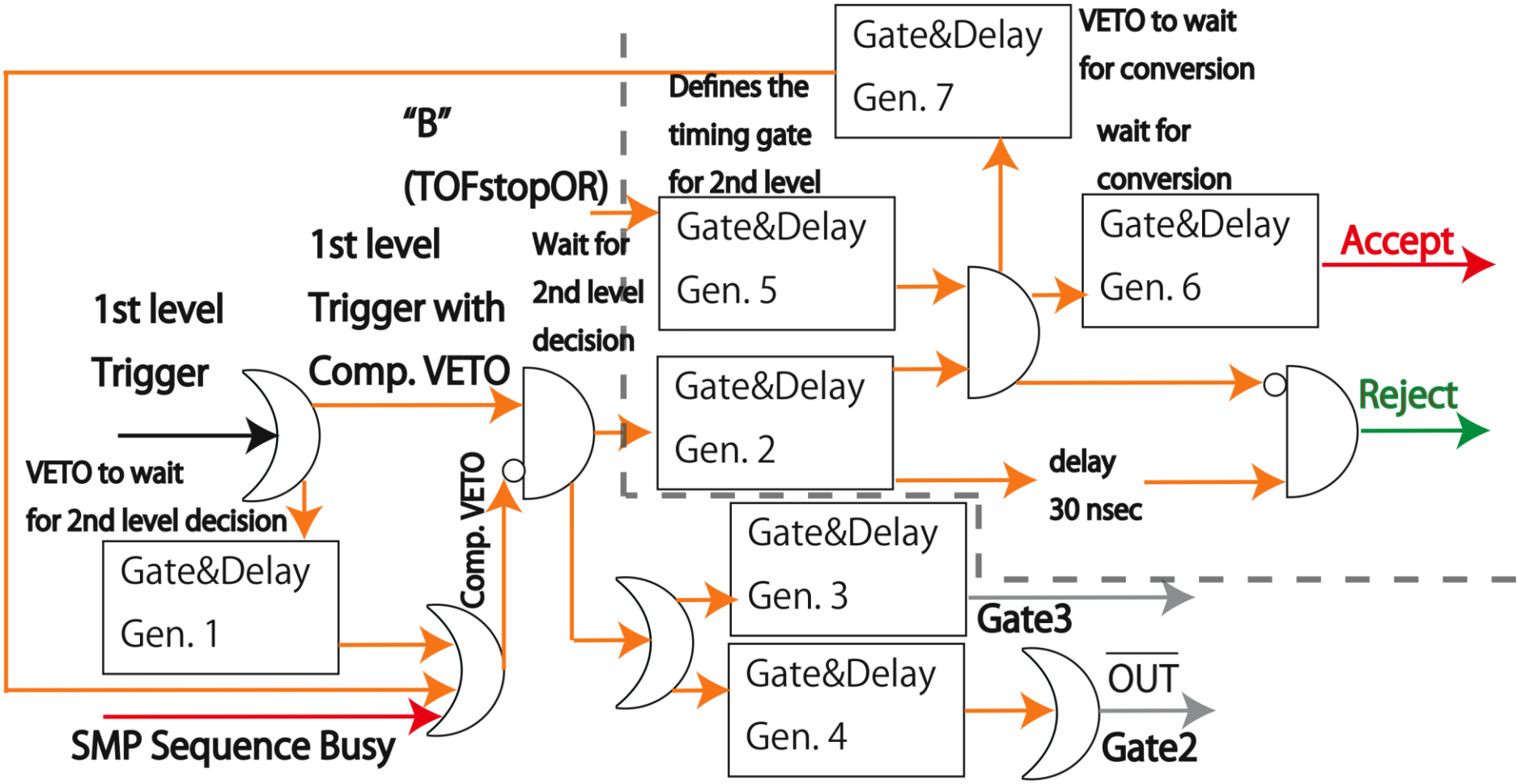
Trigger rate (s^{-1})	Measured efficiency (%) /Acquired events (s^{-1})	Calc. efficiency (%) (T_A=700 μs)
1.14×10^2	92.6 / 105	92.6
5.07×10^2	73.75 / 374	73.81
9.85×10^2	57.14 / 563	59.19
2.56×10^3	29.03 / 743	35.82
4.81×10^3	12.76 / 614	22.90



Specifications of TKO modules

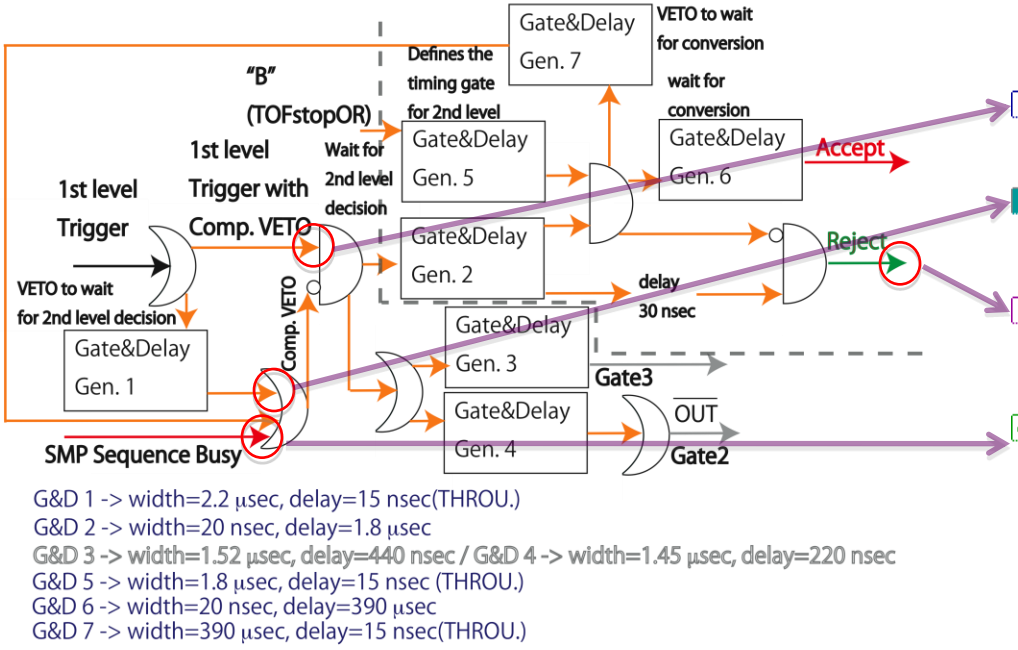
Modules /parameters	Module Clear (μs)	Conversion time (μs)
RPT-040(Dr. T, 32ch)	0.8 (gate3. gate2 can be "ON" just after the CLEAR.)	12/hit channel × 32 = 384 as the absolute max.
RPT-140 (H.R. TDC, 16ch)	0.6	5/hit channel × 16 = 80 as the absolute max.
T004 (Charge ADC, 32ch)	0.5 (0.4~0.5)	100
T005 (PH ADC, 32ch)	0.8	100
T008?(Wilkinson PH ADC, 16ch)	0.8	30
T1351 (64ch HR TDC) as a reference	1.0	90

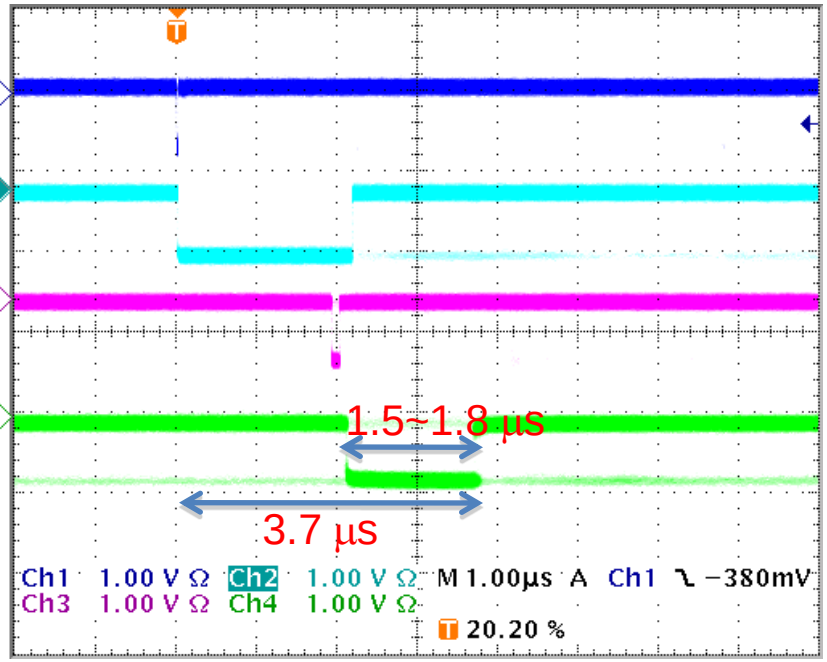
New Trigger Circuit



G&D 1 -> width=2.2 μsec, delay=15 nsec(THROU.)
G&D 2 -> width=20 nsec, delay=1.8 μsec
G&D 3 -> width=1.52 μsec, delay=440 nsec / G&D 4 -> width=1.45 μsec, delay=220 nsec
G&D 5 -> width=1.8 μsec, delay=15 nsec (THROU.)
G&D 6 -> width=20 nsec, delay=390 μsec
G&D 7 -> width=390 μsec, delay=15 nsec(THROU.)

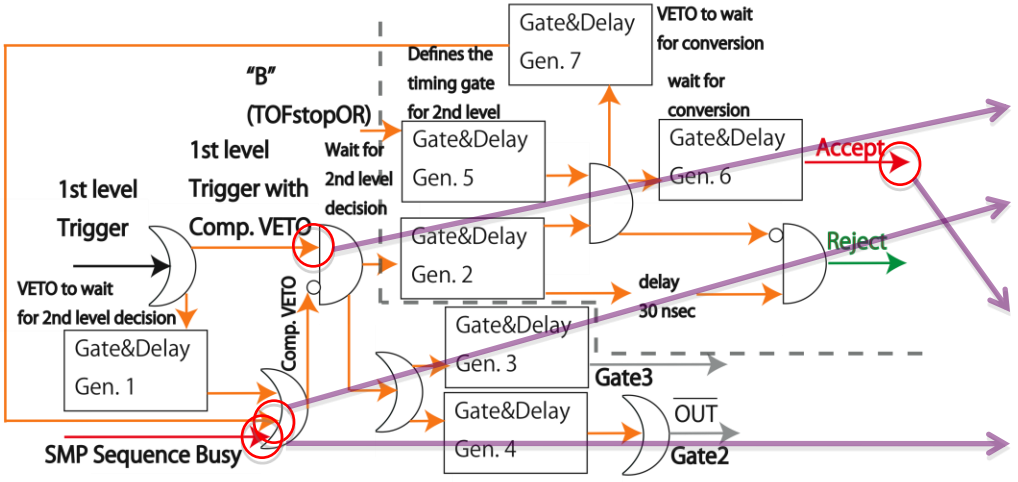
Timing Check (1)





- Dead time of "Reject" sequence : **1.5~1.8 μs**
- Depending on the delay and width of timing gate waiting for "B", overall dead time is **3.7 μs / event**.

Timing Check (2)



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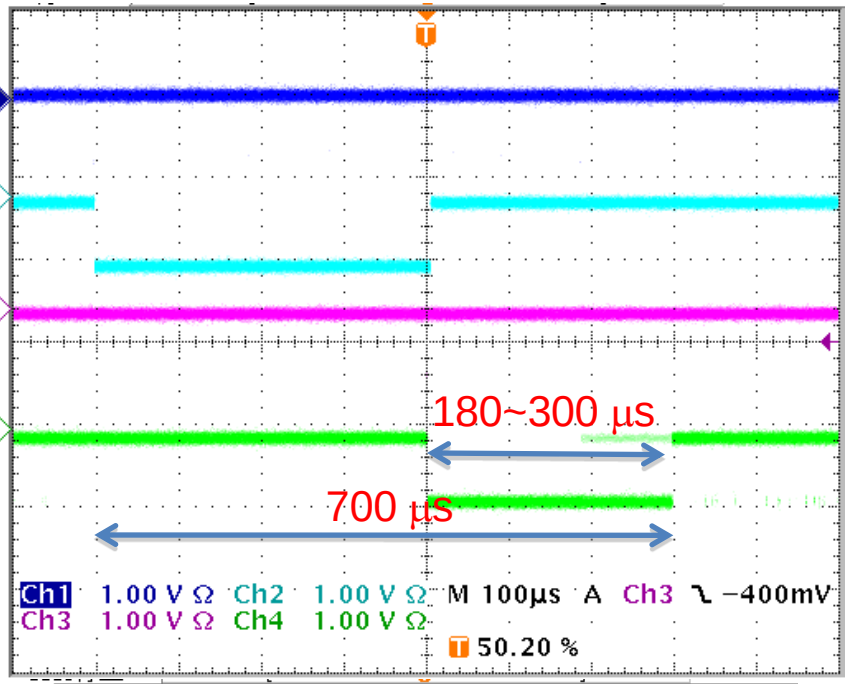

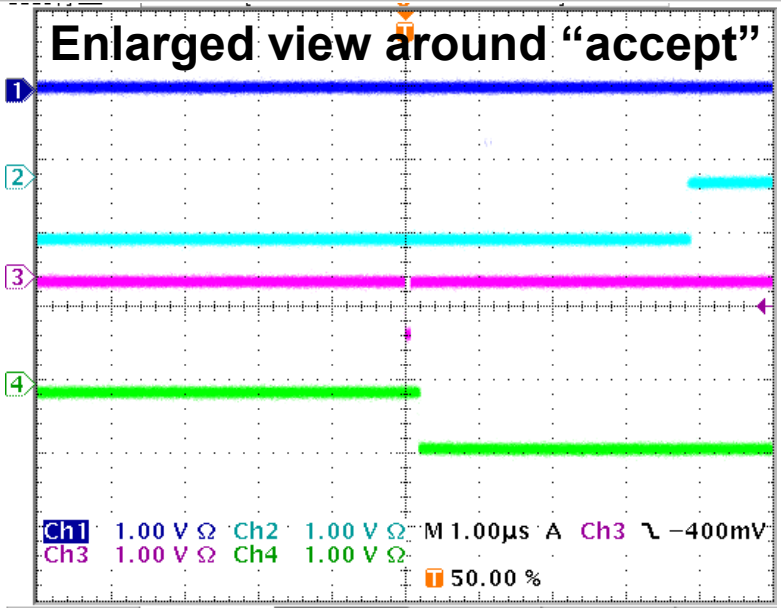

- Dead time of "Accept" sequence : 180~300 μs
- Overall dead time is 700 μs / event.

Data