September 15, 2005

Progress report of LHeII Target for E570

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Now, LHeII Target is cooled by Liq. N_2 for calibration of SDDs

< Setup >

Please refer to Fig. 1.

① 5 SDDs were attached in a cryostat. (Refer to Fig. 2, 3)
The No. 0, 1, 4, 5, 6 ports were equipped with SDD.

② The pipe which include the ^{55}Fe checking source inside was attached for calibration of the SDDs. The pipe was purged air with N_2 dry gas. (1 atm at room temp)

③ 4 holes of the down stream of the radiation shield for wiring were closed in consideration of heat input.

④ At the tip of a pipe from 1K pot, the cap was attached to the change of a target cell.

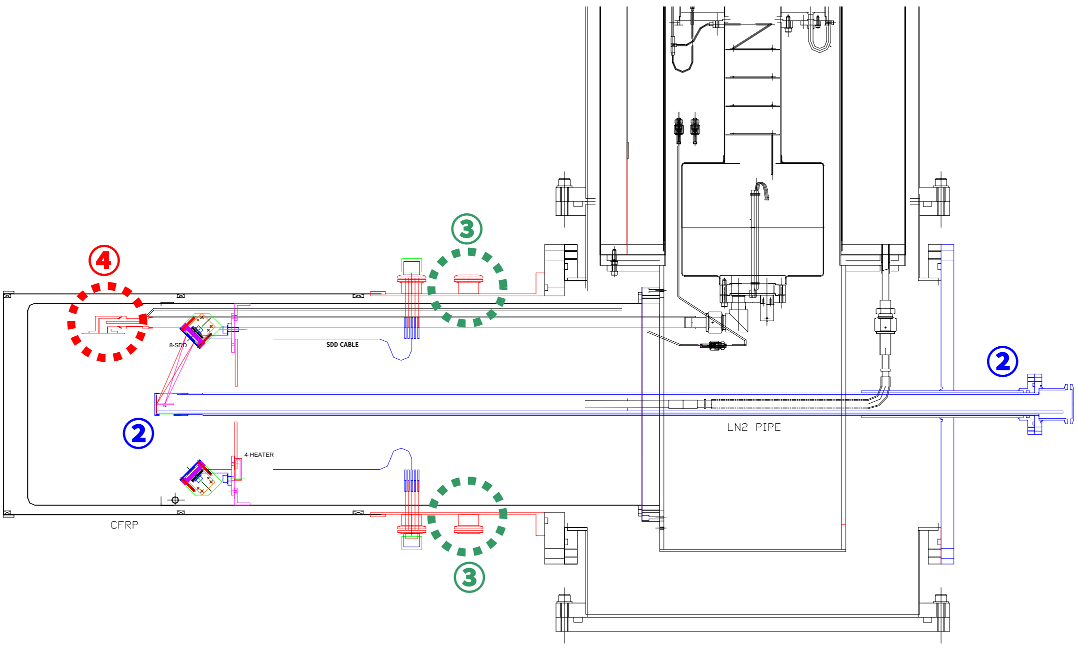


Fig. 1. Setup for SDD calibration test

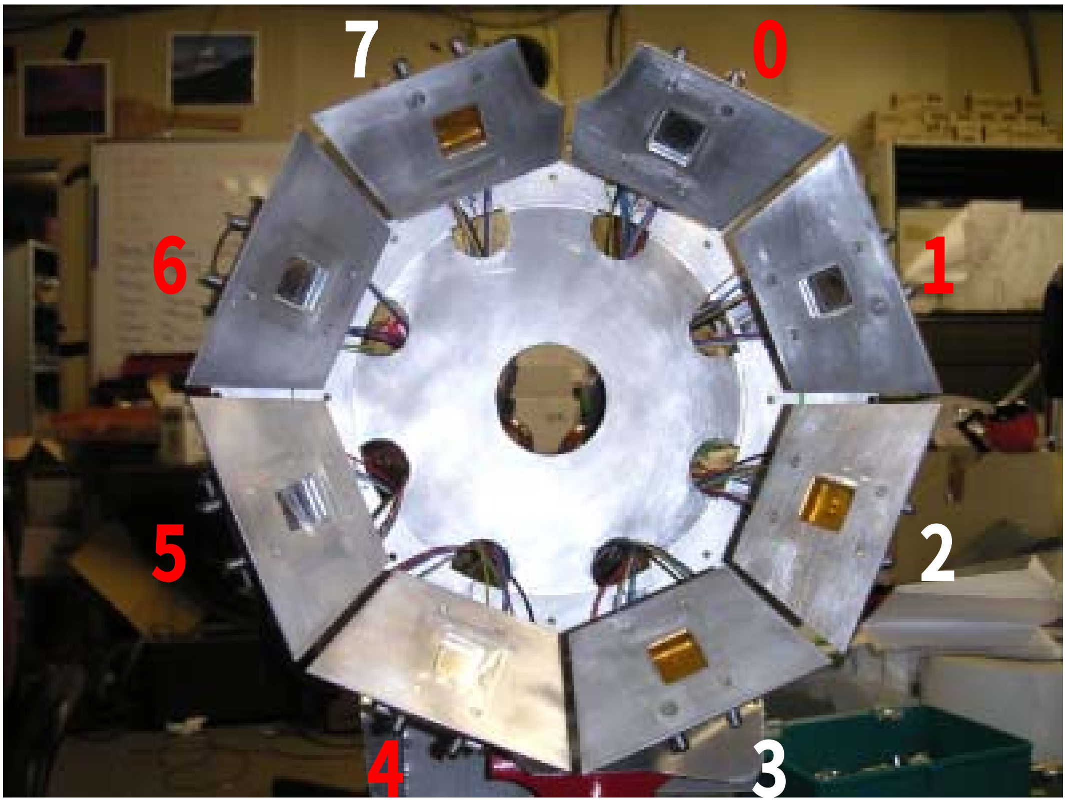


Fig. 2. Front view of SDDs


Fig. 3. Rear view of SDDs

< Test condition >

- N_2 buffer was filled with Liq. N_2. The radiation shield and SDDs were cooled by heat conduction.
- 4 K buffer was also filled with Liq. N_2.
- 1 K pot was filled with ^{4}He gas (1 atm at room temp) after vacuuming.

(It is possible to fill a liq. N_2 from 4 K buffer to 1 K part using needle valve.)

< The test result of cryogenic side >

The plot of the temperature of SDD and other parts are shown in the following Fig. 4, 5, 6.

- Temperature of SDD was ～83 K. (In the last cooling test with Liq. He, it was ～85 K .)

➔ Heat input decreased by closing 4 hole of the radiation shield.

- Temperature change of a short time like a burst was observed again.

(It may disappear, when filling in Liq. He to 4 K buffer and 1K pot.)

<The future plan to beam time>

- We will do a cooling test using Liq. He once again by final setup.

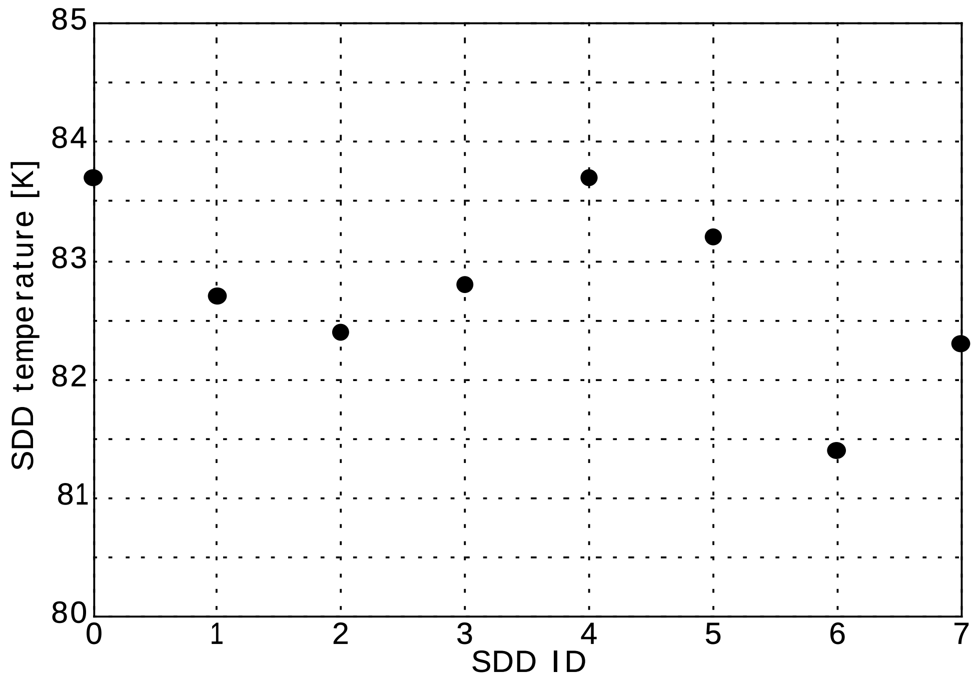


Fig. 4. Temperature of SDDs

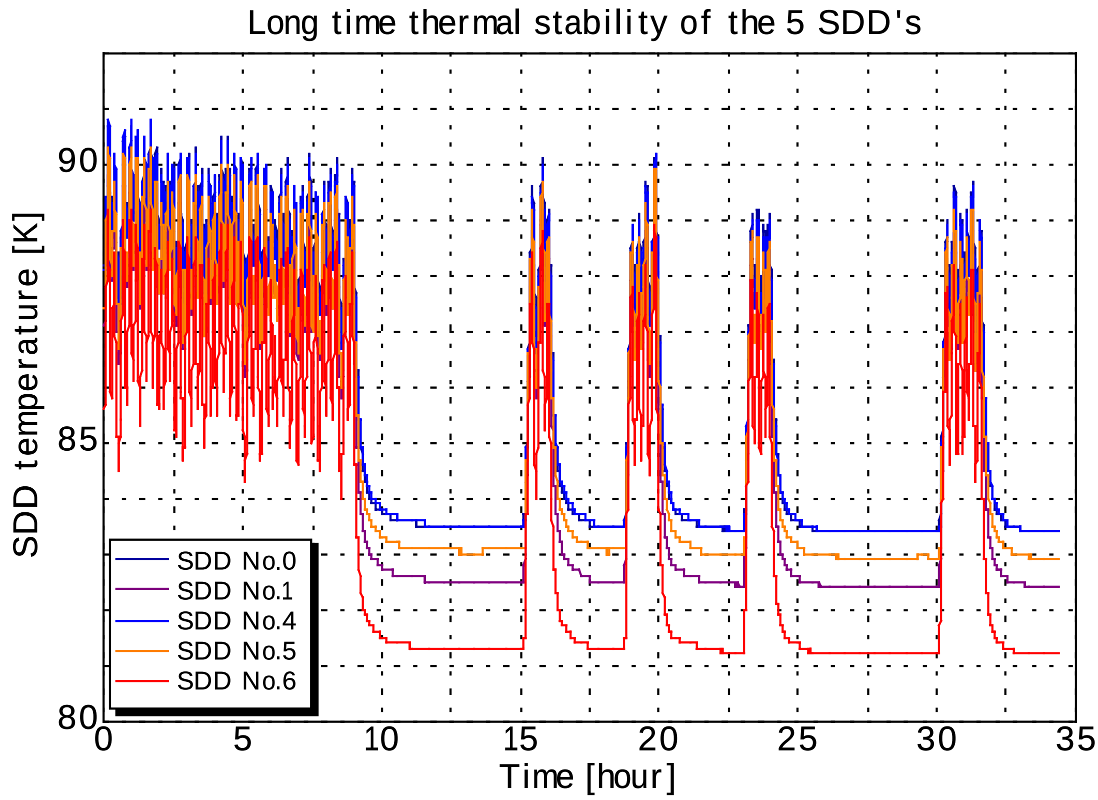


Fig. 5. Long time thermal stability of SDDs

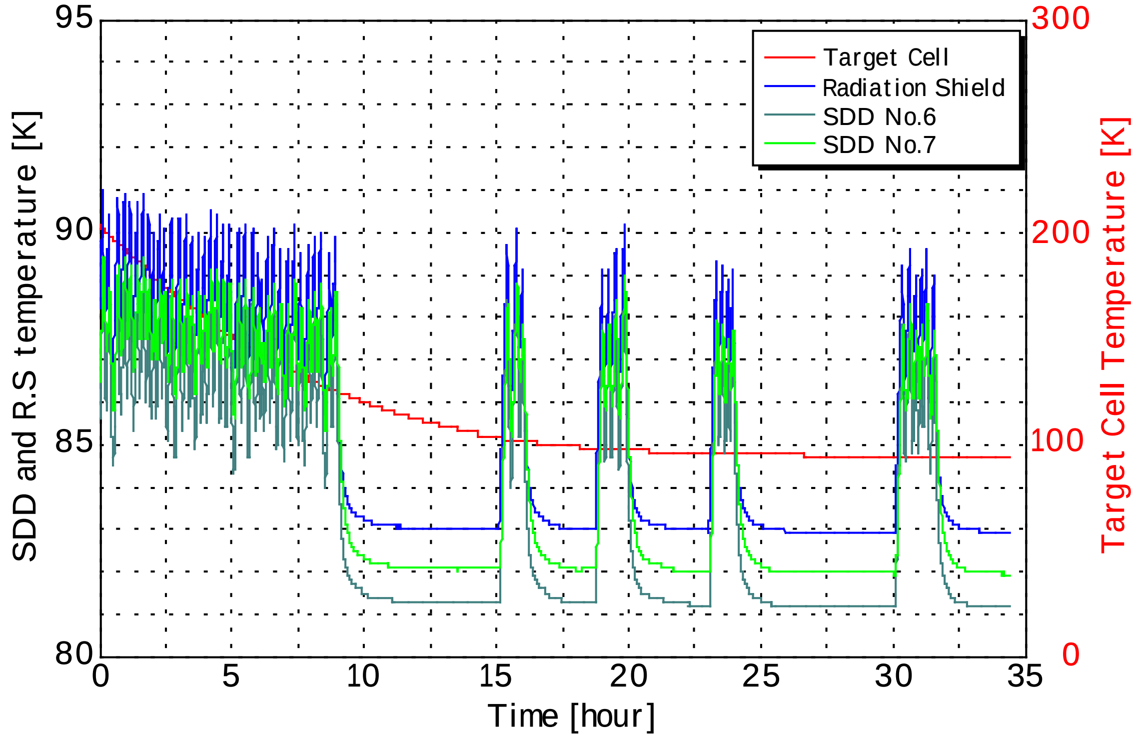


Fig. 6. Temperature of SDDs, R.S and Cell

SDD Status

Hideyuki Tatsuno

2005.9.15

1 Introduction

Now 5 SDDs (No.1, 2, 5, 6, 7) are installed at E570 setup, 2 SDDs (No.4, 8) are used for test bench cryostat, and No.3 is shipping from KETEK.

Two of the 5 SDDs No.2 and No.7 are working correctly, but others are not. Moreover the test bench is in bad form now, so No.8 working hasn't be confirmed yet.

2 SDD Status

2.1 SDD No.1

At room temperature No.1 worked correctly, but after LN_2 cooling it doesn't make any response. Maybe the inner side cable are disconnected.

2.2 SDD No.2

SDD No.2 is working correctly and its shaping-amp signal can be seen at upstairs. No.2 pre-amp out is shown in Figure 1.

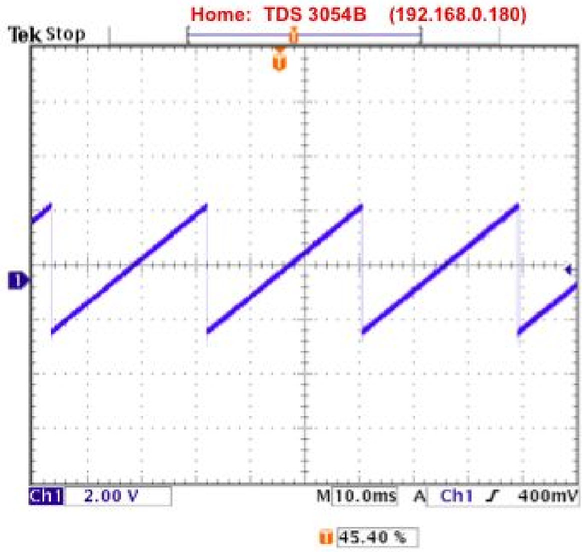


Figure 1: SDD No.2 pre-amp output.

2.3 SDD No.3

SDD No.3 is shipping from KETEK.

2.4 SDD No.4

SDD No.4 is in the test bench cryostat. It was calibrated in last week and confirmed correctly working. But recently the test bench setup is bad form, even No.4 SDD signals are suspicious like Figure 2. The shaping-amp signals have some ground noise and their pulse height are all different.

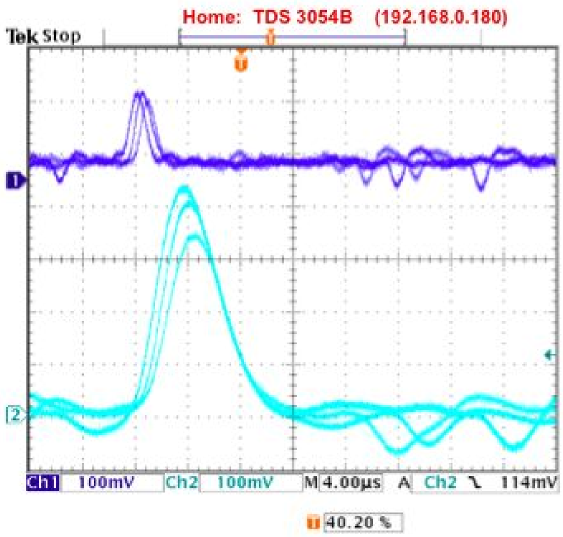


Figure 2: SDD No.4 shaping-amp signals in the test bench cryostat.

2.5 SDD No.5 and No.6

SDD No.5 and No.6 are installed in the realistic E570 setup. At room temperature they looked normal, but after LN_2 cooling the resonance was observed. No.5 and No.6 pre-amp outputs are shown in Figure 3 and Figure 4.

2.6 SDD No.7

SDD No.7 is working correctly and its shaping-amp signal can be seen at upstairs. No.7 pre-amp out is shown in Figure 4.

2.7 SDD No.8

The test bench is out of condition now, No.8 hasn't be checked correctly yet...

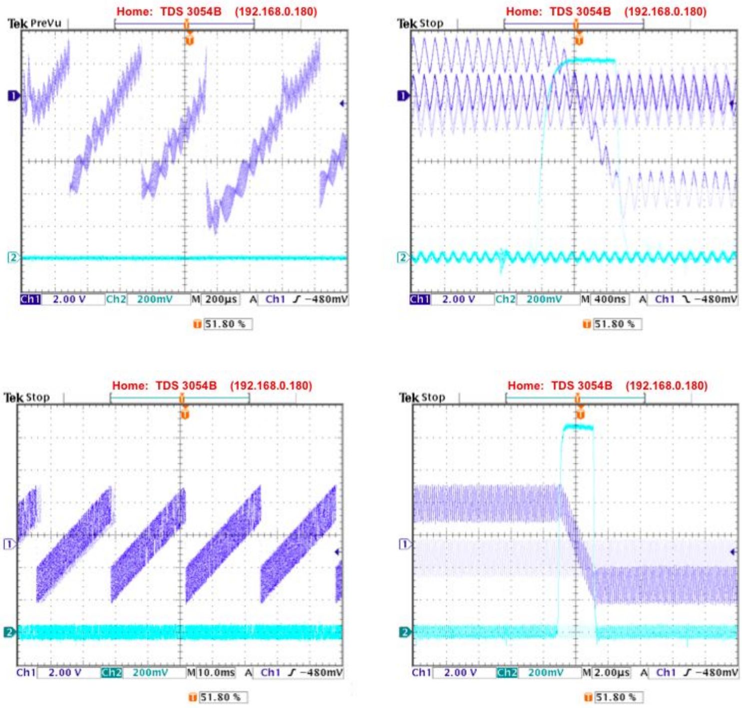


Figure 3: Up: left is SDD No.5 pre-amp output, right is with reset pulse. Bottom: left is SDD No.6 pre-amp output right is with reset pulse.

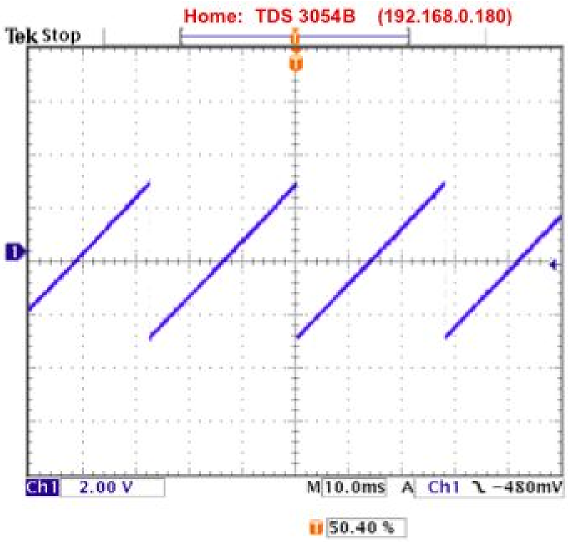


Figure 4: SDD No.7 pre-amp output.

2005/09/15 S.Okada

E570 meeting

Test for hit position dependence of "FOUT" output (CAEN N568B)

1. Collimator

Fig 1 shows a design of ^{55}Fe source collimator which could collimate to hit the X-ray with an area 0.28mm in diameter of a SDD.

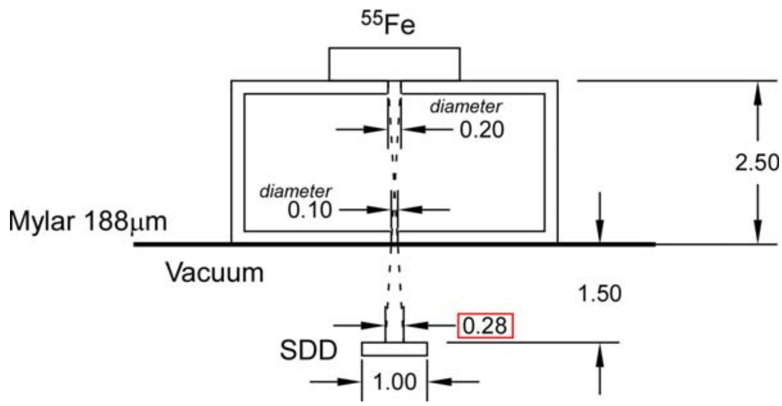


Fig 1： Schematic view of ^{55}Fe source collimator (2mm thickness aluminum)

Fig 2：Pictures of test bench setup with the collimator (left fig.) and without the collimator and a vacuum flange (right fig.)

2. Typical events

Since the event rate was extremely low due to the collimator, we took the data (pictures) event by event by using oscilloscope. 23 events for center source position and 15 events for edge position were obtained. Typical events (event#1-#4) for center source position are shown in Fig. 3. First pulse (blue line) shows “OUT” output (Shaping time 3μs); second one (light blue) shows “FOUT” output; third one shows logic pulse made by “OUT” of shaping time 0.2 μs and reset veto.

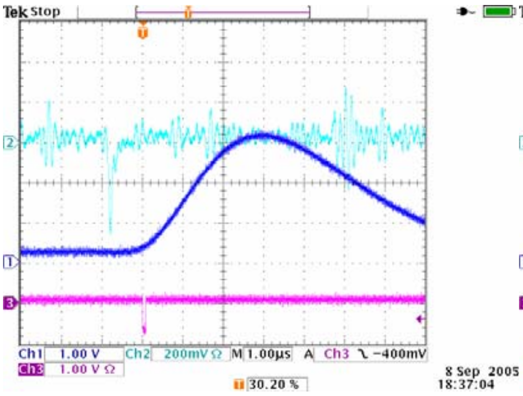


Fig 3 : Event #1 (center)

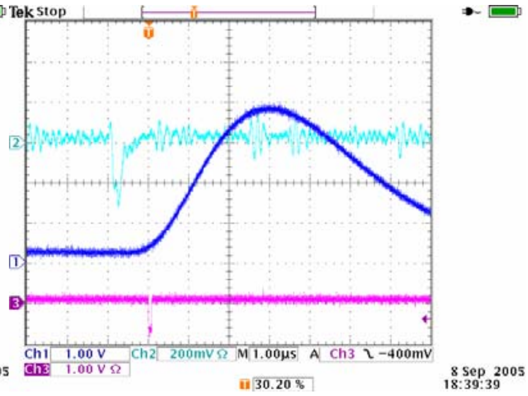


Fig 4 : Event #2 (center)

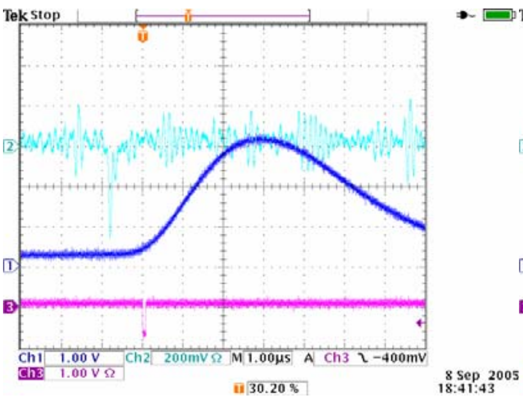


Fig 5 : Event #3 (center)

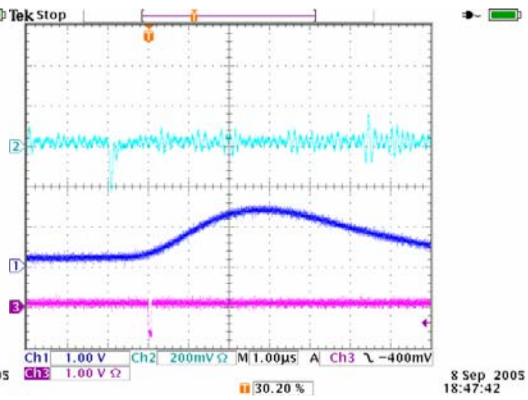


Fig 6 : Event #4 (center)

Some events were having wide width FOUT pulse such as event #2 (Fig. 4). In that case, the pulse height seems to be half compare to normal signal. (see Fig. 7)

3. Correlation between OUT and FOUT pulse height

Fig 7 shows correlation between OUT and FOUT pulse height measured by eye. Blue dots are data for center source position; pink dots are for edge. Both correlations seems to be separated. For the events of the wide width FOUT pulse, the pulse height seems to be half (yellow dots for center and green dots for edge).

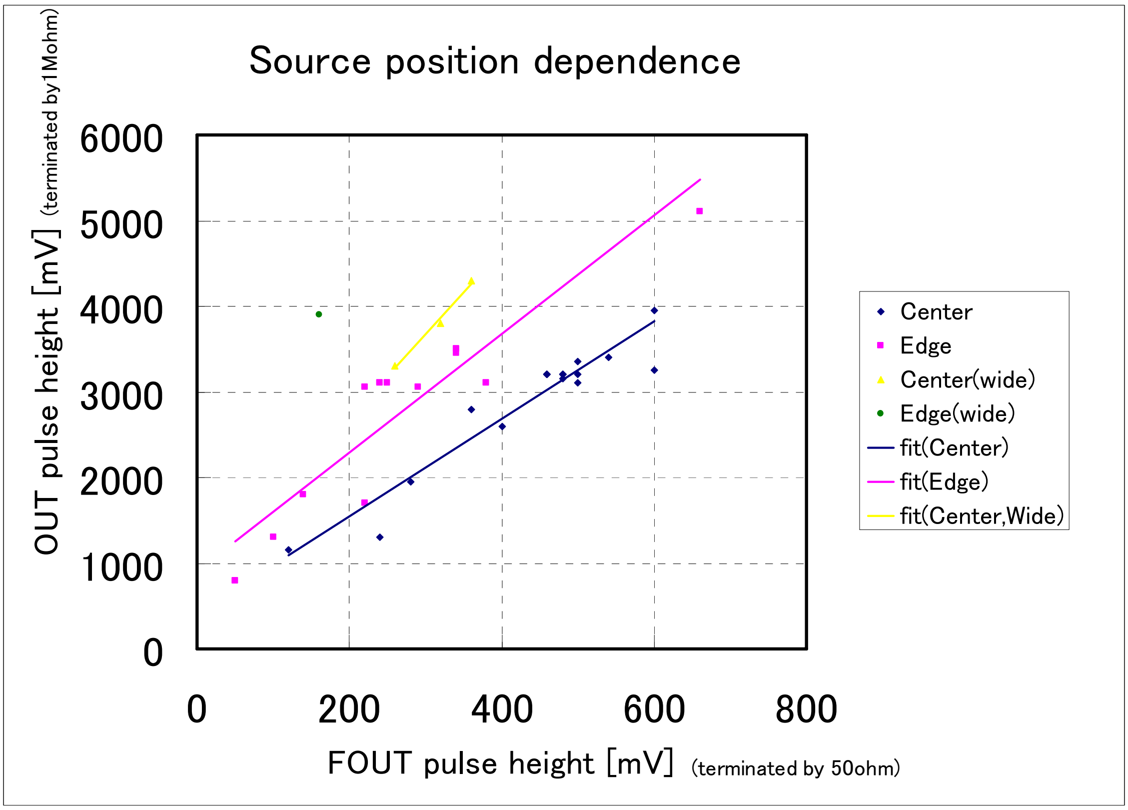


Fig 7 : Correlation between OUT and FOUT pulse height
for center and edge source position

* It should be noted that the impedance of the oscilloscope inputs for OUT and FOUT is different (OUT = 1Mohm, FOUT = 50ohm). The pulse height terminated by 1 Mohm is typically three times higher than that of 50 ohm.

^{90}Sr source test

1. Setup

To check the correlation between TDC and FOUT/OUT, we performed timing test using electron source ^{90}Sr. The setup is shown in Fig 8.

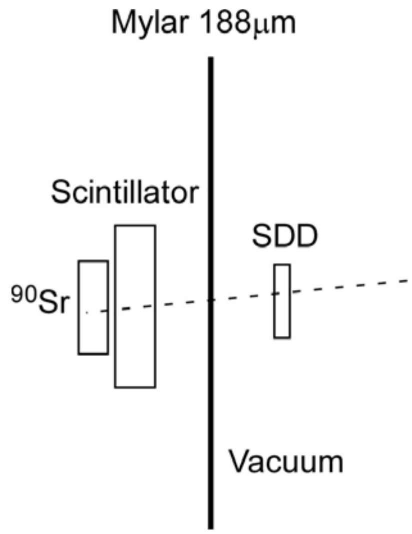


Fig 8 : ^{90}Sr source test setup

2. Result

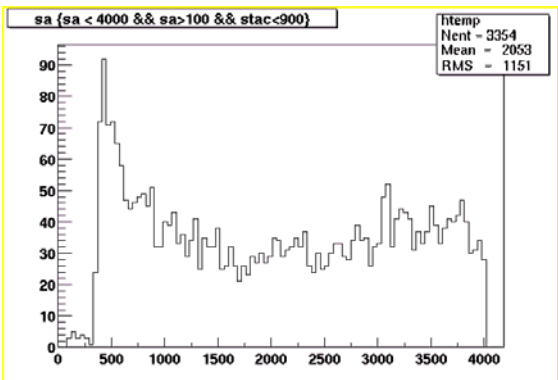


Fig 9 : ADC spectrum of OUT

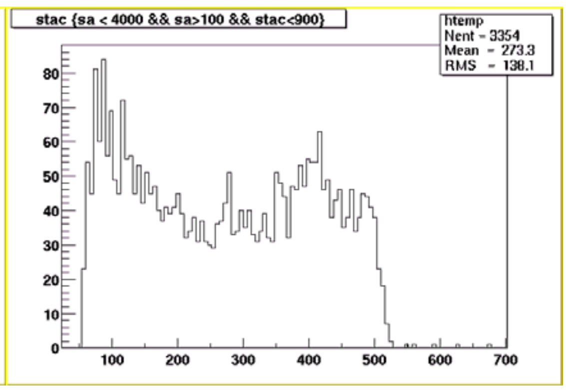


Fig 10 : ADC spectrum of FOUT

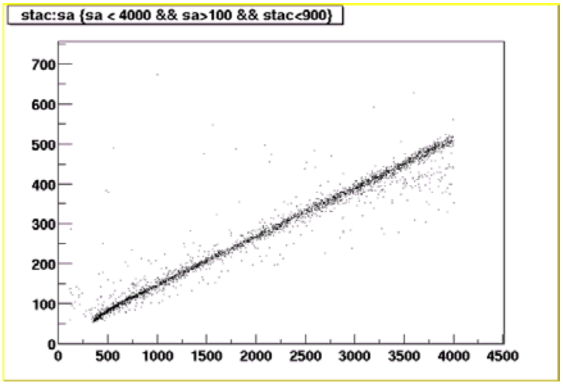


Fig 11 : correlation between OUT and FOUT

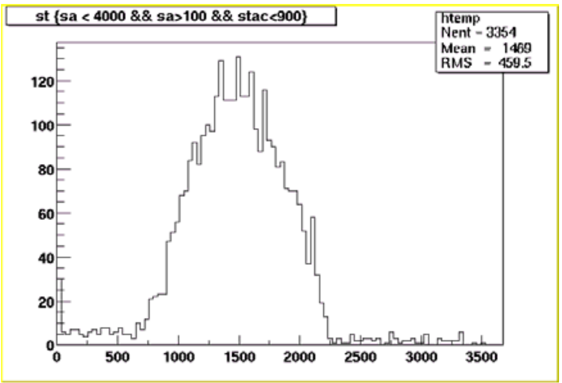


Fig 12 : TDC spectrum

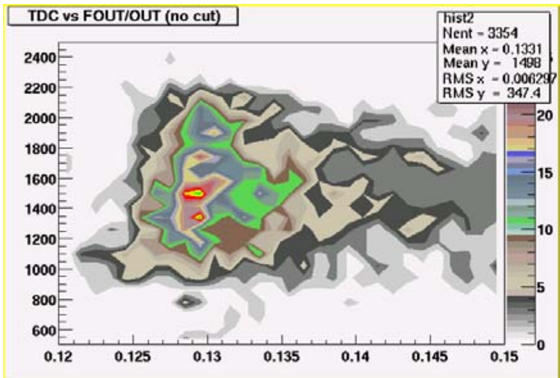
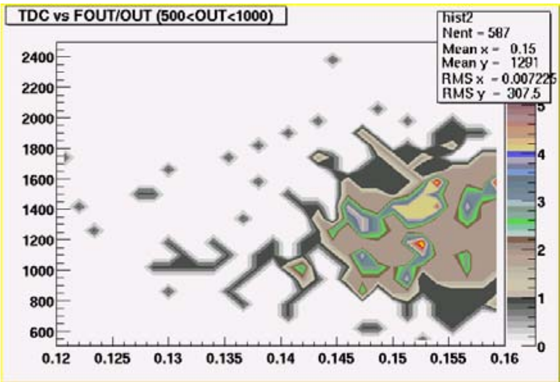


Fig 13 : TDC vs FOUT/OUT (no cut)



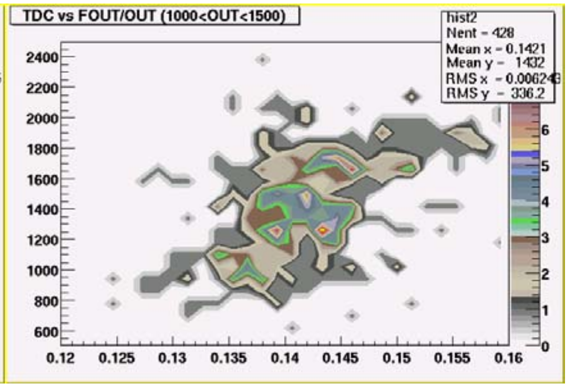
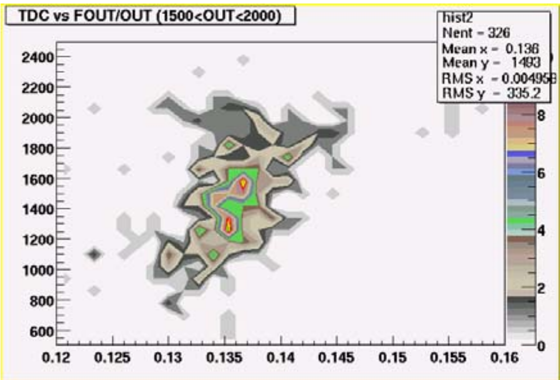


Fig 14 : cut 500<OUT<1000

Fig 15 : cut 1000<OUT<1500



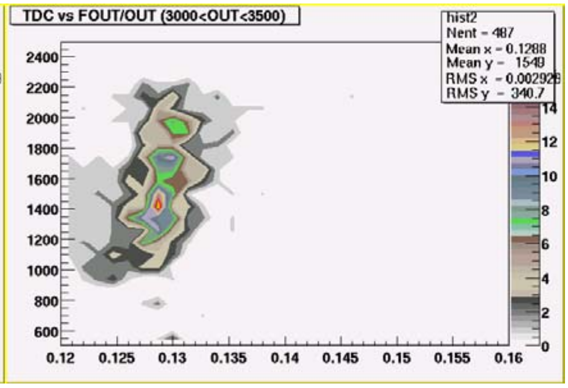
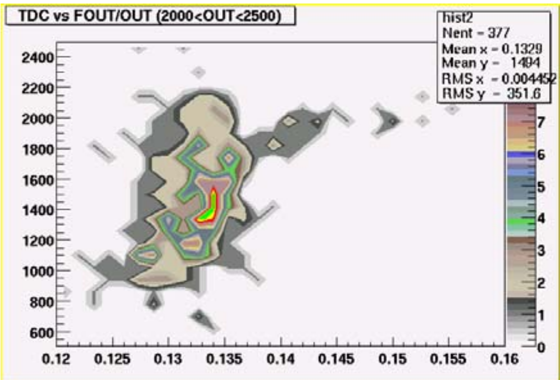


Fig 16 : cut 1500<OUT<2000

Fig 17 : cut 2000<OUT<2500



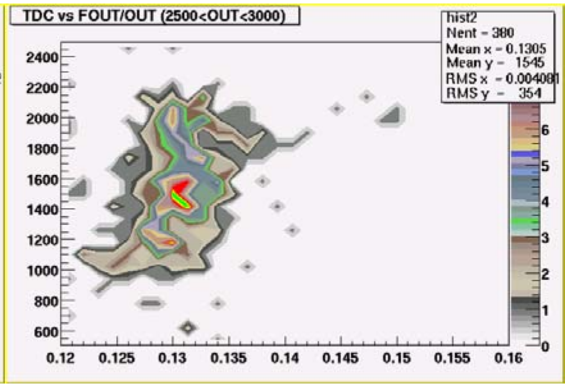


Fig 18 : cut 2500<OUT<3000

Fig 19 : cut 3000<OUT<3500

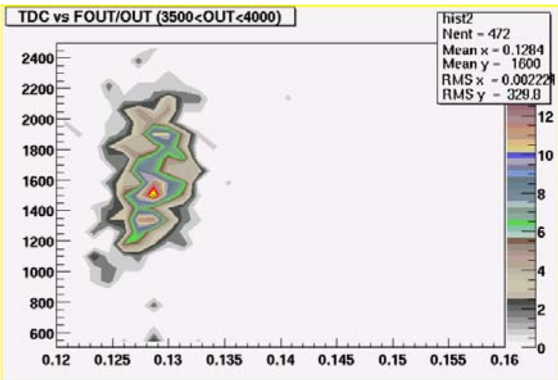


Fig 20 : cut 3500<OUT<4000

Results of the ADC nonlinearity measurements

Tomoichi Ishiwatari and Berti Juhasz

Measurement of the differential nonlinearities

Principle of the measurement

The differential nonlinearity (DNL) of the ith channel (i.e. ith bin) is defined as the deviation of the actual width of the channel from the ideal width of that channel. The latter is simply the full range of the ADC divided by the number of channels.

The usual way the measure the DNL is to feed the ADC with a series of pulses with amplitudes uniformly distributed between zero and the total range of the ADC. If all channels have the same width, all channels will have the same number of counts. However, if some of the channels have different width (i.e. nonzero DNL), then these channels will have more (less) counts if their with if larger (smaller).

Actual measurement

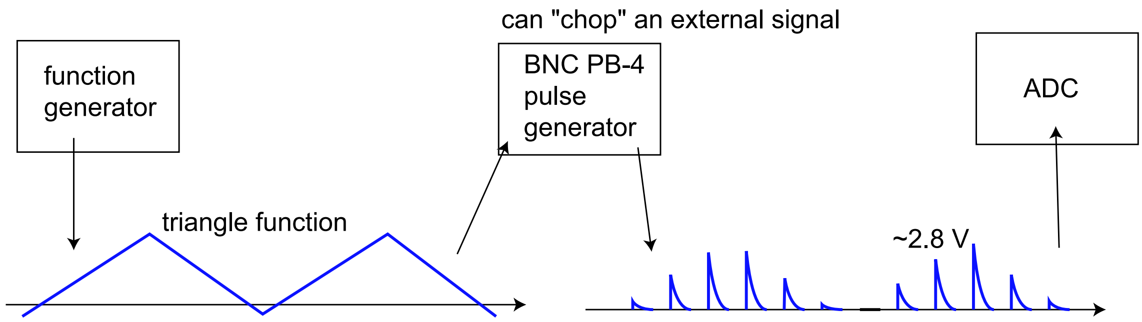


Figure 1: Principle of the differential nonlinearity measurements.

To produce the necessary pulse series, we used a function generator which had a triangle wave function output with a frequency of 200 Hz. This was fed into a pulse generator BNC BP-4 borrowed from SMI in Vienna. The pulse generator "chopped" this input at a rate of ∼1 kHz and produced single pulses at as an output. The height of a pulse is in principle proportional to the height (voltage) of the triangle function at the time of the pulse generation. These pulses were then fed into one of the 16 channels of an ADC. Figure 1 summarizes this procedure.

A typical measured ADC nonlinearity spectrum (i.e. number of counts vs. channel number) is shown in Fig. 2. Unfortunately, there is a strange structure in the spectrum (and in all spectra). This is most likely due to the small, continuous (i.e. not random) spikes in the output of the function generator (see Fig. 3). The spikes appear at the zero-crossing point of the triangle function.

It can also be seen that the spectrum is not flat but it has a slope, which suggested an ADC nonlinearity. The red line is the result of a fit of the function $N(1 + Sx)$, where x is the channel number, N is a normalization factor, and S is the slope. The problematic region is excluded from the fit. To test whether the slope is really caused by an ADC nonlinearity, one can decrease the maximum amplitude of the input pulses. If the slope is due to the nonlinearity of the ADC, then the resulting spectrum (continuous blue line in Fig. 4) will have the same slope as the original one (dotted line). However, if the slope is due to the nonlinearity of the input pulses, then the slope should increase (continuous red line).

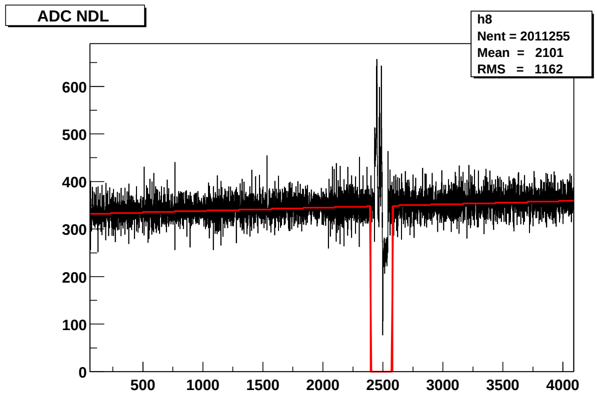


Figure 2: Measured nonlinearity spectrum of channel 7 of the ADC in slot 12.

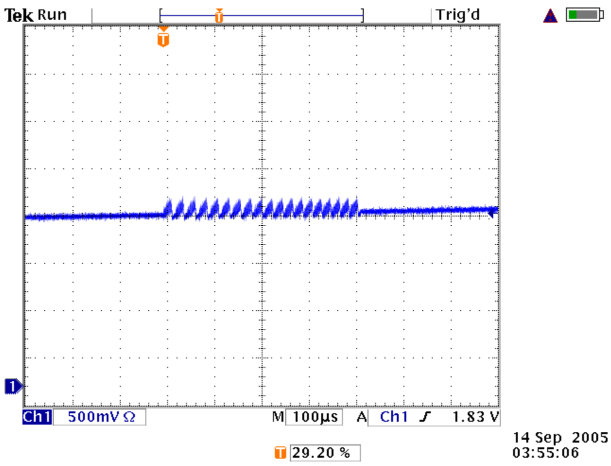


Figure 3: Oscilloscope screen capture of the function generator output.

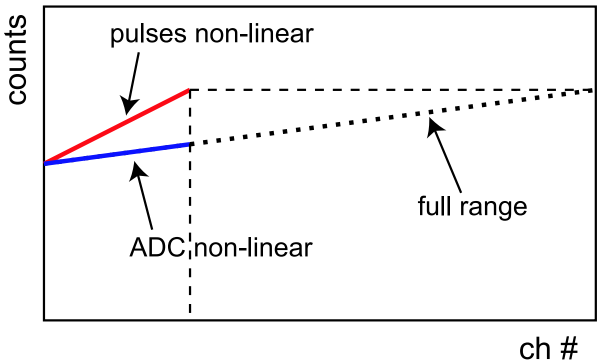


Figure 4: What can happen when one decreases the maximum amplitude of the input pulses? Dotted line: original spectrum. Continuous blue line: new spectrum if the slope is due to ADC nonlinearity. Continuous red line: new spectrum if the slope is due to the nonlinearity of the input pulses.

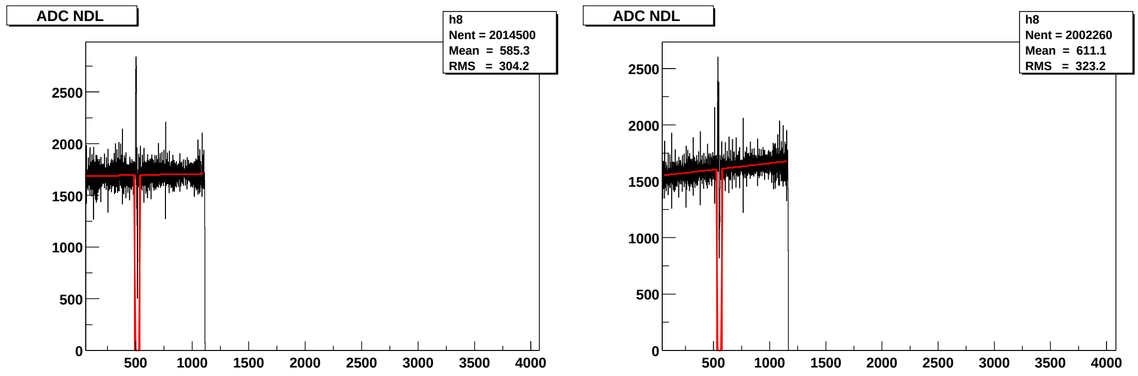


Figure 5: Effect of decreasing the voltage of the pulse series on the same channel as in Fig. 2. Left side: changing the voltage with the multi-dial. Right side: changing the voltage with the attenuator switch.

First, we used the multi-dial on the pulse generator to decrease the output voltage. This resulted in the spectrum on the left side of Fig. 5. The slope of this spectrum is actually smaller than that of the original spectrum, which suggested that we found a real ADC nonlinearity.

However, since “paranoia is the physicist’s best friend”, a few days later we made another test, but this time we used one of the attenuation switches on the pulse generator to decrease its output by a factor of 5. The result of this measurement is shown on the right side of Fig. 5. One can clearly see that this time the slope became much larger, suggesting that the slope is due to the nonlinearity of the pulses.

An explanation to the observed contradiction can be the following. Back at SMI, we tested our method with another function generator, which could only produce a triangle function at $\sim$1 kHz or higher frequency. We found that this is too fast for the pulse generator, and its output doesn’t follow the input voltage. In other words, the rate of change of the input voltage was too high. The function generator here was operated at 200 Hz, at its lowest frequency. However, this might still be too fast for the pulse generator, which caused a slope. When we used the multi-dial to decrease the voltage, we actually decreased the rate of change, because the dial decreases the input signal *before* it is processed (chopped and shaped). Since the rate of change became smaller, the signal became more acceptable for the pulse generator, and its output became more linear, and the slope decreased. However, the attenuation switch decreases the voltage *after* processing, therefore the nonlinearity of the output remains the same.

The bottom line is that this function generator is probably too fast, and we will need a much slower ($\sim$1 Hz or below) function generator for the final nonlinearity measurements after the run.

Measurement of the integral nonlinearities

Principle of the measurement

The integral nonlinearity (INL) at the ith channel (i.e. ith bin) is defined as the total deviation of the actual response function of the ADC from the ideal response function. The integral nonlinearity is the sum of the differential nonlinearities up to that channel.

The measurement of the INL is quite simple: a few pulses of the same and precise known voltage are fed into the ADC. This produces a sharp peak in the spectrum. By repeating this procedure with different pulse heights, we can plot the channel numbers vs. the input voltage.

This way we essentially obtain the actual response function of the ADC at a few points.

Actual measurement

We used the pulse generator alone to produce the pulses. The output voltage of this device is supposed to be very linear i.e. the output voltage should follow the setting of the multi-dial very strictly: according to the specifications, the integral nonlinearity is ±0.005%, the differential nonlinearity is ±0.03%, while the amplitude jitter is 0.001% rms (10 ppm).

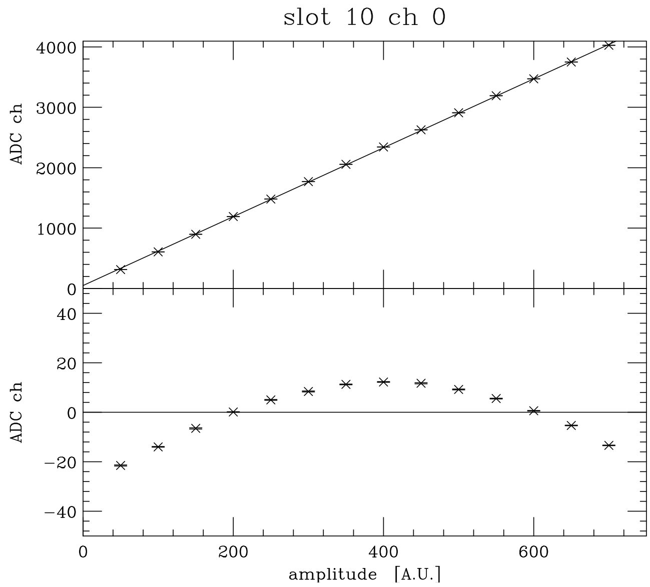


Figure 6: A typical measured response function (channel 0 of the ADC is slot 10).

The upper part of Fig. 6 shows a typical response function that we obtained. The X axis is the setting of the multi-dial. In the lower part, the deviations of measured points from a fitted linear function are drawn. The maximum INL occurs around the middle of the ADC range, and it is appr. 0.5%.