2005/08/24 S.Okada and H.Tatsuno

E570 meeting

Test for CAEN N568B module

1. Reducing noise

FOUT (Fast OUT) signal which we showed in the last meeting was very noisy. After that, we tried to reduce the noise and succeeded in reducing noise of SDD preamp signal by shielding the connection part of hermetic port as shown in Fig 1.

Fig 2 shows outputs of CAEN N568B module: FOUT and OUT with 0.2μs shaping time. We could more clearly see the FOUT signal than previous one, but it is still noisy…

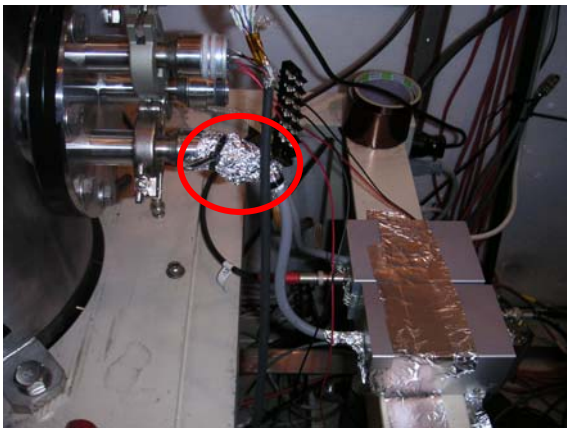


Figure 1 : Cable shielding of the connection parts of hermetic port.

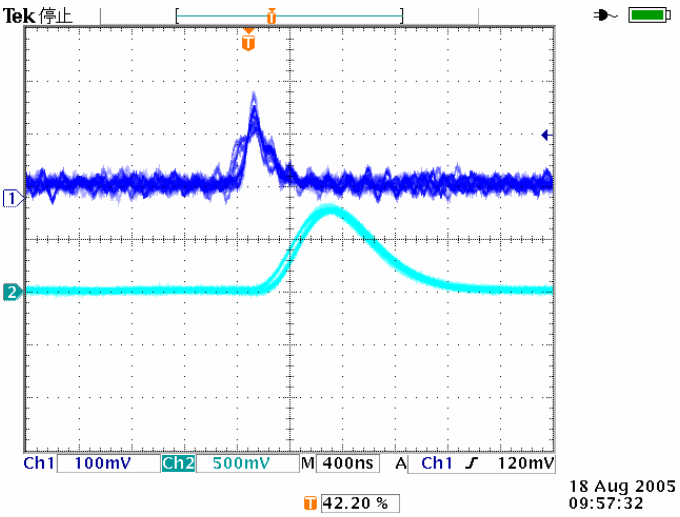


Fig 2 : CAEN N568 outputs … 1: FOUT signal, 2: OUT signal (shaping time 0.2μs)

2. Rise time with differentiating circuit

Fig 3 shows SDD rise time triggered by output of differentiating circuit; preamp out and output of differentiating circuit. The rise time is about 200ns.

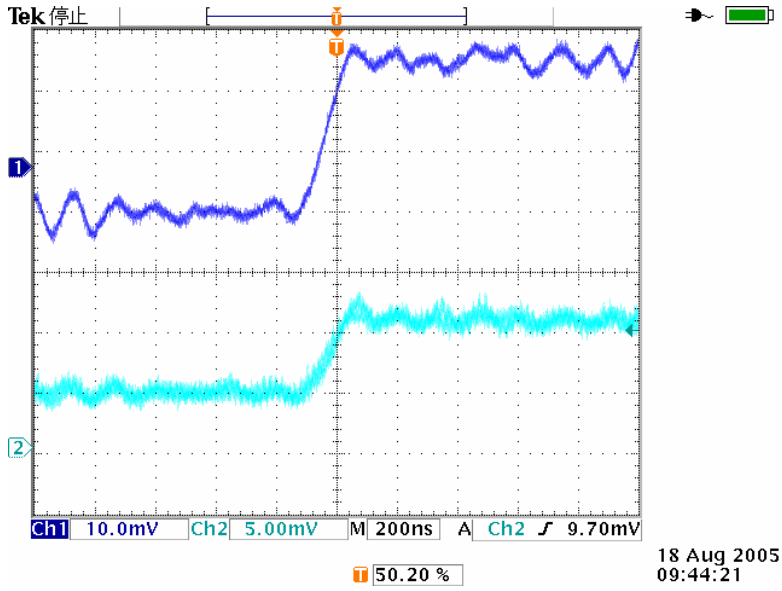


Fig 3 : SDD rise time… 1:preamp output, 2:Output of differentiating circuit

3. Cross talk check

We checked cross talk between neighboring channels of CAEN N568B. Fig 4 and Fig 5 show the outputs of channel #1, #2, #3 and #4 for a x-ray signal from ^{55}Fe source and a reset pulse respectively. The cross talk was seen for reset signal, but it was 20mV signal for about 10V signal of reset pulse. → There was only 0.2% cross talk.

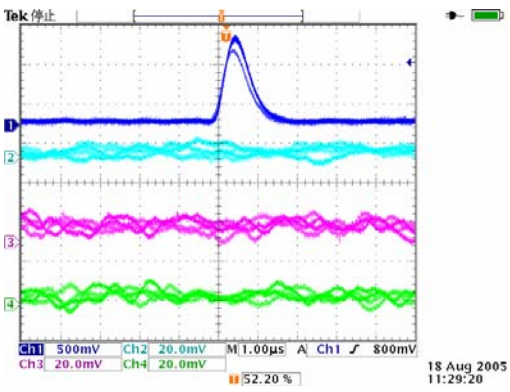


Fig 4 : x-ray signal from ^{55}Fe source

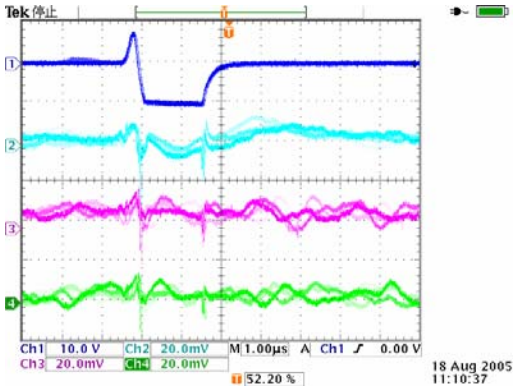


Fig5 : Reset signal

Signal cable from SDD to preamp

Now we are checking SDD output signal with realistic cable length between SDD and preamp using shielding cable. With this condition, strange resonance was seen as shown in Fig 6 and 7.

Realistic cable length : 57cm (from SDD to hermetic port) + 15cm(from hermetic port to preamp)
Previous test bench : 15cm(from SDD to hermetic port) + 30cm(from hermetic port to preamp

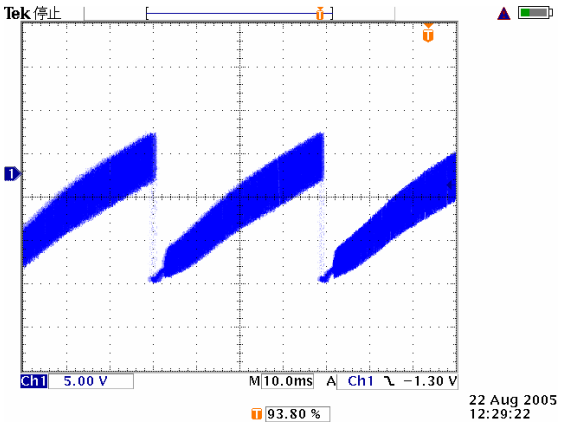


Fig 6 : Preamp output (wide range)

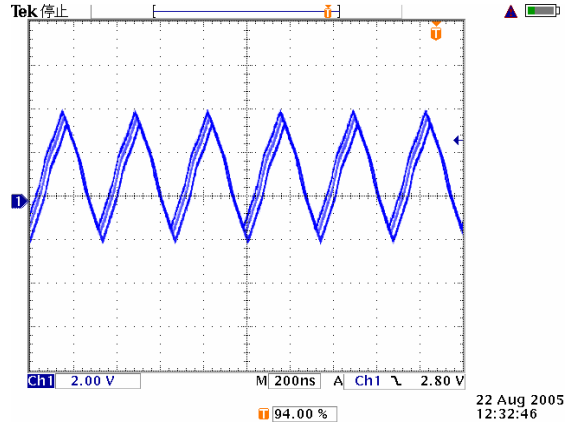
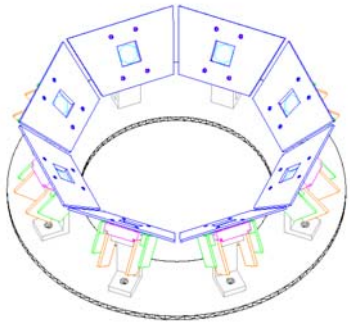


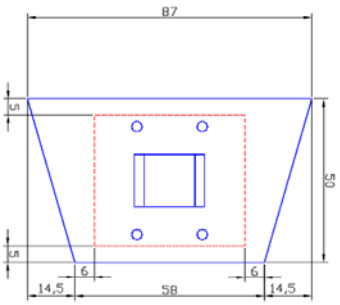
Fig 7 : Preamp output (narrow range)

Preparation status of E570

SDD

- SDD： All eight SDDs is ready. We will finish the operation check for all SDDs in next week.
- Preamp：
  - Preamp boxes and supports will be delivered tomorrow from CI company.
  - Though we bought two backup preamps from KETEK, we have lost one preamps at KEK (now we are still finding...) and found that one preamp was broken. Since we received only two preamps (not three preamps) from SMI when Eberhard brought us three SDDs, we have therefore only seven usable preamps. So one preamp is lacking and we have no backup preamps. SMI group will send us one preamp which is their backup. Moreover, they said the broken preamps can be repaired by SMI side.
- SDD support
  - Aluminum holder and G10 board will be delivered tomorrow.
  - Front face cover of SDD is made by pure aluminum plate (99.999%) to avoid x-rays from impurity of the aluminum holder. (Nilaco AL-013606 … size 3.0*100*300mm (¥33,500)). The cover is enlarged in order to avoid x-rays from backside of SDDs shown in following figure. (The red dashed line shows original Al cover size.)





Electronics

- Timing filter amp
  - We have borrowed TFA (timing filter amp) “ORTEC???” from Tamura-san. Now we are checking the module.
  - We also borrowed Fast Amp which is used for wire chamber at old KEK experiment and is designed by Taniguchi-san.

- Gate generator

  We need 8 + 8 + 1 + 1 + 1 = 19 channels. (see circuit diagram)

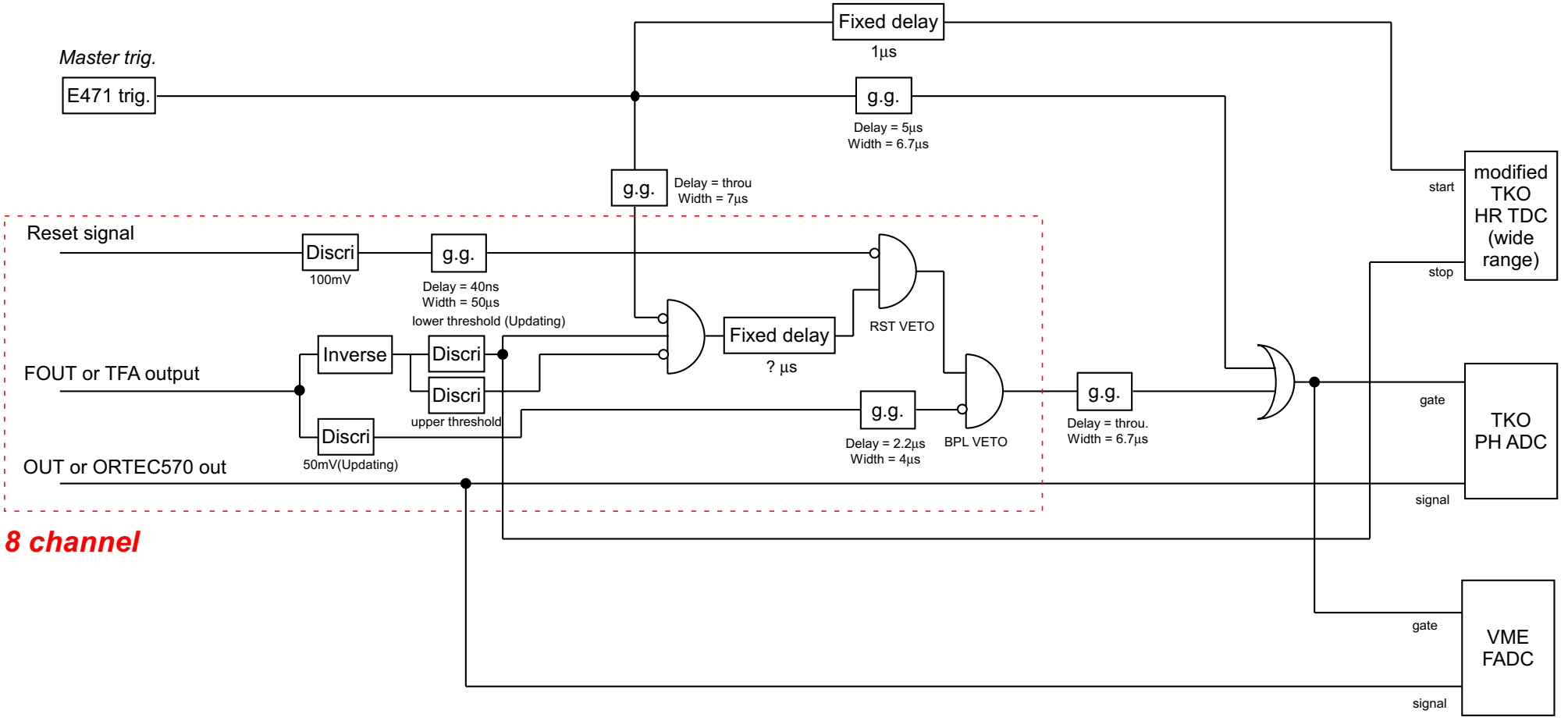
  Now we have …

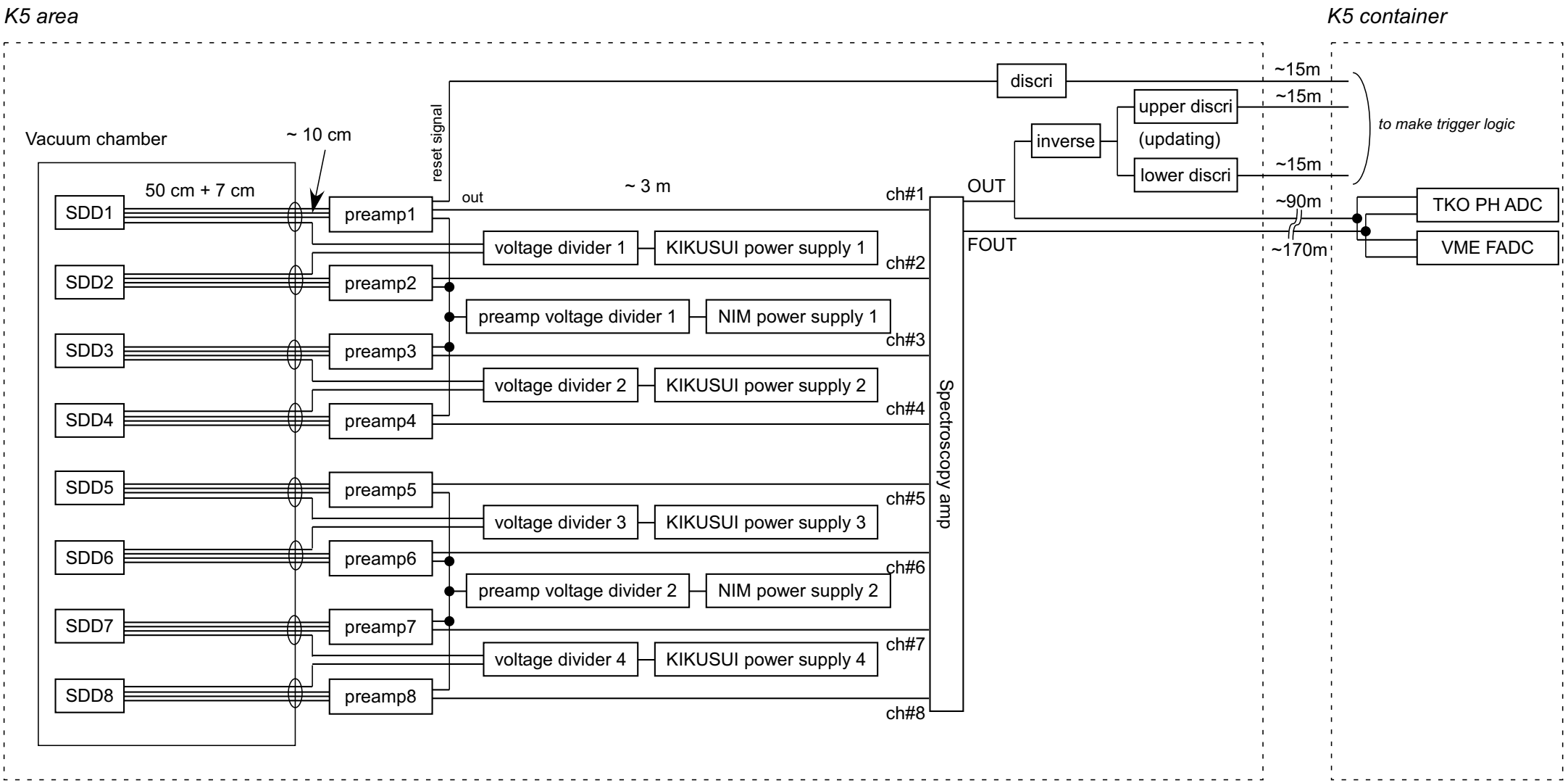
  - 2 channel gate generator : 12 moudules
  - 4 channel gate generator : 1 module
  - 8 channel gate generator : 2 modules (We ordered Techno company.)

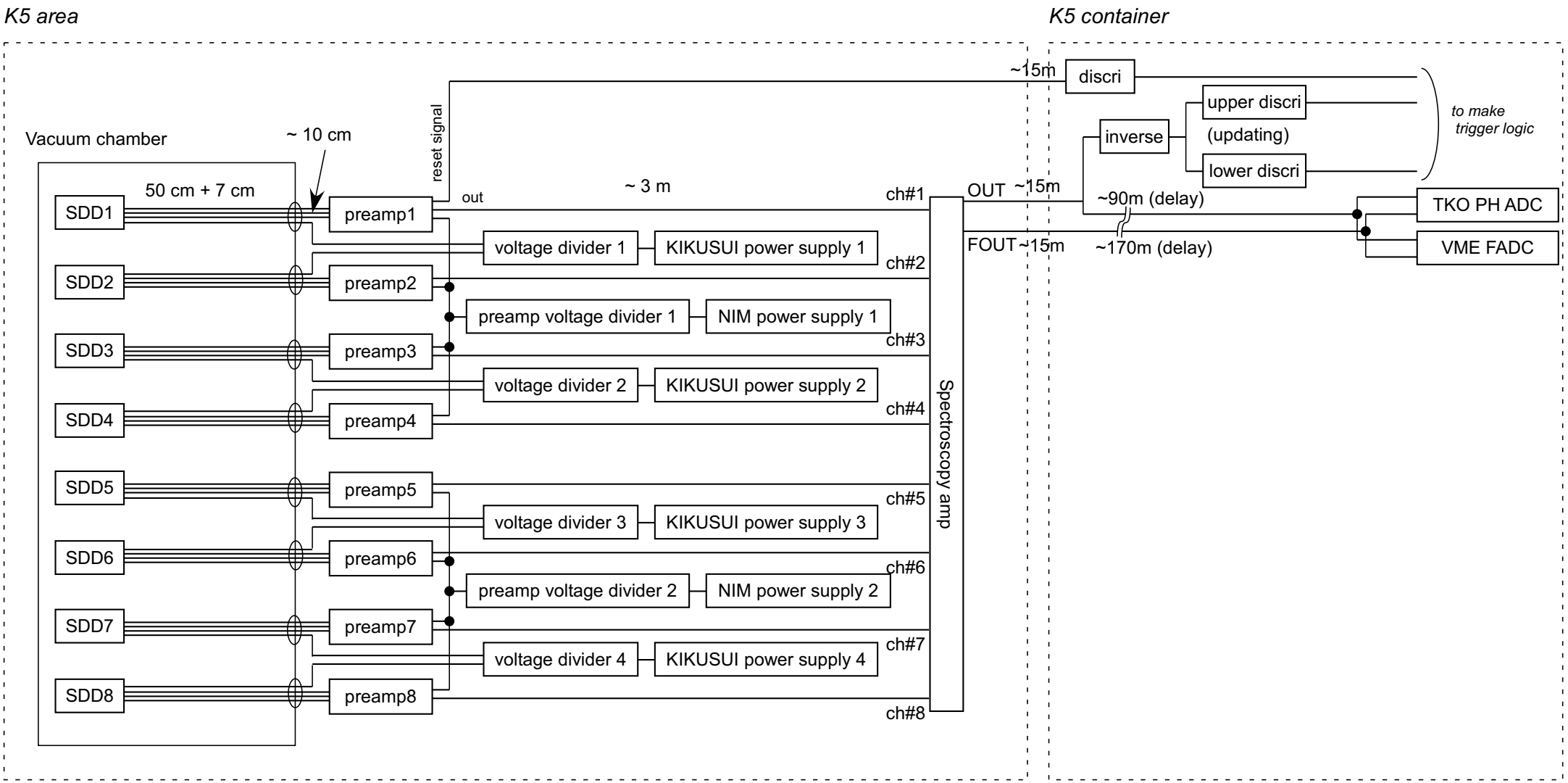
  → 42 channels

Temperature control

- We succeeded in reading the data from LakeShore 340 and operating the system with GPIB by Sato-san's help.


Master trig.
E471 trig.
Fixed delay
1µs
g.g.
Delay = 5µs
Width = 6.7µs
g.g.
Delay = throu
Width = 7µs
modified
TKO
HR TDC
(wide
range)
start
stop
Reset signal
Discri
100mV
g.g.
Delay = 40ns
Width = 50µs
lower threshold (Updating)
RST VETO
Fixed delay
? µs
FOUT or TFA output
Inverse
Discri
Discri
upper threshold
Discri
50mV(Updating)
g.g.
Delay = 2.2µs
Width = 4µs
BPL VETO
g.g.
Delay = throu.
Width = 6.7µs
gate
TKO
PH ADC
signal
OUT or ORTEC570 out
gate
VME
FADC
signal
8 channel


K5 area
K5 container
Vacuum chamber
~ 10 cm
50 cm + 7 cm
reset signal
out
~ 3 m
SDD1
SDD2
SDD3
SDD4
SDD5
SDD6
SDD7
SDD8
preamp1
preamp2
preamp3
preamp4
preamp5
preamp6
preamp7
preamp8
voltage divider 1
KIKUSUI power supply 1
preamp voltage divider 1
NIM power supply 1
voltage divider 2
KIKUSUI power supply 2
voltage divider 3
KIKUSUI power supply 3
preamp voltage divider 2
NIM power supply 2
voltage divider 4
KIKUSUI power supply 4
ch#1
ch#2
ch#3
ch#4
ch#5
ch#6
ch#7
ch#8
Spectroscopy amp
OUT
FOUT
discri
inverse
upper discri
(updating)
lower discri
~15m
~15m
~15m
~90m
~170m
to make trigger logic
TKO PH ADC
VME FADC


K5 area
K5 container
Vacuum chamber
~ 10 cm
50 cm + 7 cm
reset signal
out
~ 3 m
SDD1
SDD2
SDD3
SDD4
SDD5
SDD6
SDD7
SDD8
preamp1
preamp2
preamp3
preamp4
preamp5
preamp6
preamp7
preamp8
voltage divider 1
KIKUSUI power supply 1
preamp voltage divider 1
NIM power supply 1
voltage divider 2
KIKUSUI power supply 2
voltage divider 3
KIKUSUI power supply 3
preamp voltage divider 2
NIM power supply 2
voltage divider 4
KIKUSUI power supply 4
ch#1
ch#2
ch#3
ch#4
ch#5
ch#6
ch#7
ch#8
Spectroscopy amp
OUT
FOUT
~15m
~15m
~90m (delay)
~170m (delay)
discri
upper discri
(updating)
inverse
lower discri
to make
trigger logic
TKO PH ADC
VME FADC

23/Aug/2005

>> E570 実験 Flash ADC 読み出しスキーム <<

Flash ADC は基本的に、SDD のデータを取得するための装置なので、
トリガは SDD のセルフトリガとなる. 但し以下の条件が必須となる.

条件
・SDDトリガが TKO 側にアクセプトされたイベントは、F-ADC もアクセプトする
・TKO 側はいじらない.

手法
・F-ADC は 25 MHZ 駆動 128 点サンプリング = 5.12 マイクロ秒読み出し.
自動スタート、ストップ入力の、遅延トリガモード.

・フリートリガの数は、
E549トリガ → 850 triggers/spill
SDDトリガ → 200 triggers/spill
但し、150 triggers/spill は校正用フォイルからのイベント.
50 triggers/spill 程度は E549 トリガと同期する.

・同期する場合 SDD トリガは、X 線と同期する粒子の入射がつくる
E549 トリガに対して、4 マイクロ秒遅延して発生し、SDD のアナログ
シグナルに対して、0.5 マイクロ秒程度早く発生する.

・F-ADC の復帰時間(dead time)は 8 x 40 ns = 320 ns (要確認)

・F-ADC のトリガ条件は図の通りで
極めて稀だが、直前のセルフトリガによって、TKO アクセプトイベントが
取得できなくなる可能性を考慮する必要がある.

・F-ADC 側のステータスを、TKO の TDC を用いてステータス情報として記録
する必要がある.

同期を取る方法
・10 分の単位は
PC の時計を Buffer switch ごとのヘッダーに記録する.

・1 秒の単位は
Buffer switch ごとに、VME スケーラーの値を記録する.
入力は、10 kHz クロック (= 100 ms).
VME スケーラーは、F-ADC TKO 両サイドに設置し、双方とも
スレーブに設定. F-ADC 側 DAQ スタートと同時にF-ADC 側の
インタラプトレジスタから、Reset + Start の送信を行う.
Preset Scaler を利用して 10 分に一度、同時リセットを行う.

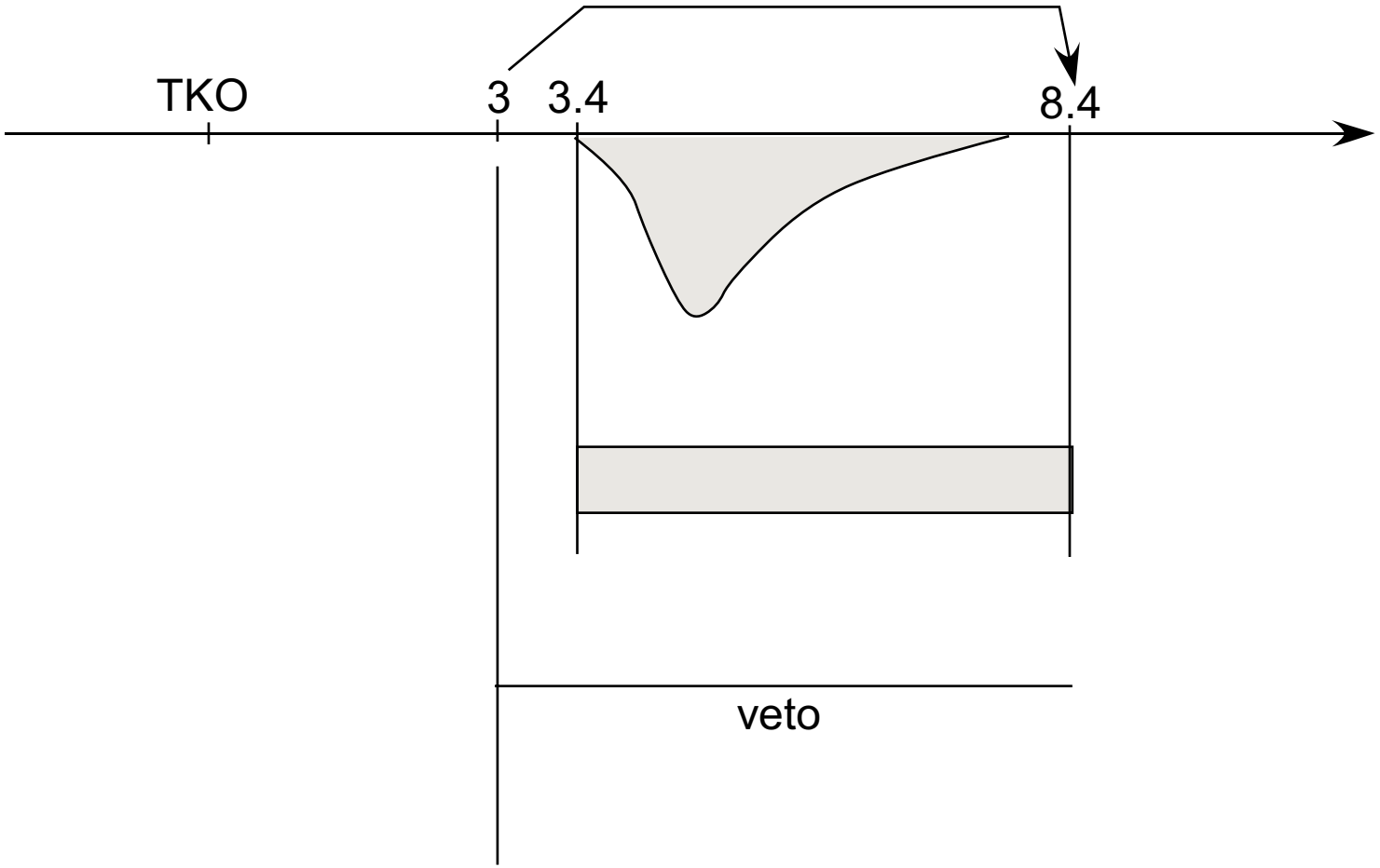
・TKO 側をいじるのを最小限にしたいので、TKO のバッファスイッチ信号を
F-ADC 側にフィードして、インタラプトレジスタにて割り込みを使って
F-ADC 側のバッファスイッチを行う.
(但し、ここで F-ADC 側は dead time が発生するはず. また、
バッファスイッチのタイミングは完全には同期しない)

・スピルごとに、バッファスイッチを行うかどうか、どうやって行うかは未定.

・TKO 側は、REF (TKO スケーラー)モジュールを用いて、TKO アクセプトイベント
の間隔を計測する. (<100 マイクロ秒程度の誤差)

・F-ADC 側は、40 ns 程度の分解能で、イベント間隔を計測可能.

・スピルの最初に、同期専用のコントロール信号を発生して、TKO と F-ADC の
両方を同時に空読みさせ、このイベントを基準に、イベントを再構築する.



Flash ADC の復帰には 8x40= 320 ns 必要
よって、必須な条件は SDD の セルフトリガから
第一サンプリング点までに 320 ns 以上の時間差が
あること. Flash ADC は AutoStart Sampling または
Gate chaining mode を使用する.

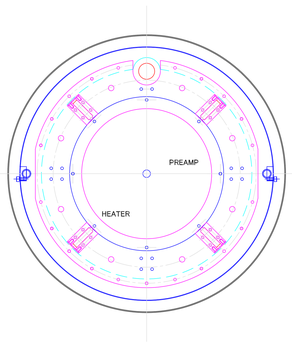
トリガは (E549 + 4 μs ∩ SDD)∪ (SDD ∩ !VETO)

E570 Preparation Schedule

Aug. 24, 2005

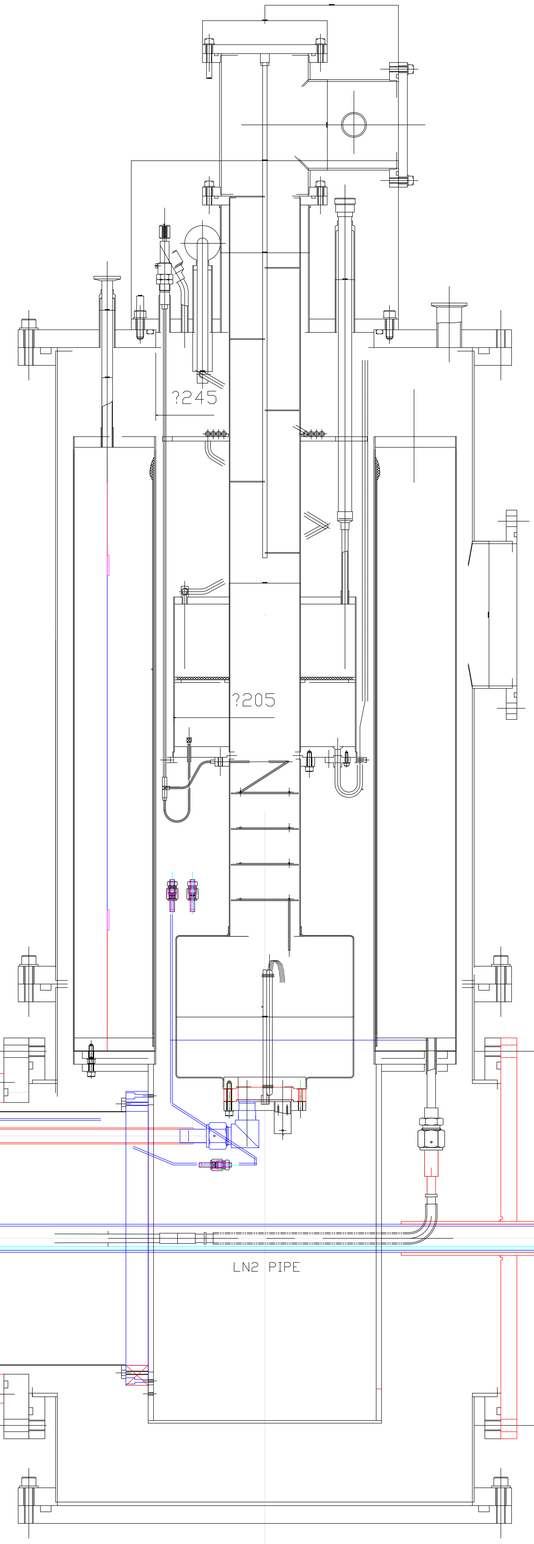
DATE		Schedule	Status	To Do	Comments
Aug.	15		Assemble	Keithley2700 Wire/Soft Install	
	16		Assemble	LN2 Dewar 200L	
	17		Vacuum Test	Leak Test	
	18		LN2 Cooling Test	LabView Soft, Heater Control Test	
	19			LabView Soft, Heater Control Test	
	20	No Electricity (8-20)	Warm Up		
	21	No Electricity (8-20)	Vacuum Pump		
	22		LN2 Cooling Again	LN2 Dewar 100L	LN2 CE(N-CH)
	23		L-He Cooling Test (1)	L-He Consumption Test	L-He transfer
	24	E570 Meeting		LakeShore 340 Test	L-He transfer
	25		Warm Up		
	26	L-He Order by 17:00	Disassemble/Assemble		
	27		Assemble	M.L.I. on the Copper Pipe, Cell	
	28		Assemble	M.L.I. on the Connectors, Cables	
	29	No Cooling Water	Vacuum Test	LN2 Dewar 200L	
	30	No Cooling Water	LN2 Cooling		
	31	No Cooling Water	L-He Cooling Test (2)	L-He Consumption Test	L-He transfer
Sep.	1			LakeShore 340 Test	L-He transfer
	2	L-He Order by 17:00	Warm Up	L-He 1000 --> Floor	
	3	Open House Preparation	Warm Up		
	4	**KEK Open House**			
	5		Disassemble/Assemble	**Cap with Pure-Al**	**Shield Tape**
	6		Assemble	**8 SDD Set w Shield Tape**	**8 SDD**
	7		Assemble	**Mylar+Source Pipe Assemble**	**Source Parts**
	8		Assemble	**Rt100 Set Near Heater**	
	9	L-He Order by 17:00	Vacuum Pump	LN2 Dewar 200L	
	10		LN2 Cooling	LabView Soft, Heater Control Test	
	11			SDD Test / (Cell, Cone)	
	12		**8 SDD TEST**	SDD Test / (Cell, Cone)	
	13		**with SOURCE**	SDD Test / (Cell, Cone)	LN2 Dewar 100L
	14			SDD Test / (Cell, Cone)	L-N2 transfer
	15			SDD Test / (Cell, Cone)	
	16	L-He Order by 17:00		SDD Test / (Cell, Cone)	
	17		Warm Up		
	18				
	19	**JPS/APS**	Disassemble/Assemble	**Pure-Al in the Cell**	**Ni/Ti Foil**
	20	**JPS/APS**	Assemble	**Cell Heater + Cable + PS**	
	21	**JPS/APS**	Assemble	**Ni/Ti on the Cell**	
	22	L-He Order by 17:00	Assemble	**Cone**	
	23		Assemble	**Cone + Ni/Ti**	
	24				
	25				
	26		Vacuum Pump	LN2 Dewar 200L	
	27		LN2 Cooling	L-He 1000 --> Area	
	28	**BEAM ON**	L-He Cooling		L-He transfer
	29				L-He transfer
	30	L-He Order by 17:00		LN2 Dewar 100L, Transfer	L-He transfer
Oct.	1				L-He transfer
	2				L-He transfer
	3				L-He transfer
	4		**EXPERIMENT**	LN2 Dewar 100L, Transfer	L-He transfer
	5				L-He transfer
	6				L-He transfer
	7	L-He Order by 17:00			L-He transfer
	8			LN2 Dewar 100L, Transfer	L-He transfer
	9				L-He transfer
	10				L-He transfer
	11				L-He transfer
	12			LN2 Dewar 100L, Transfer	L-He transfer
	13				L-He transfer
	14	L-He Order by 17:00			L-He transfer
	15				L-He transfer

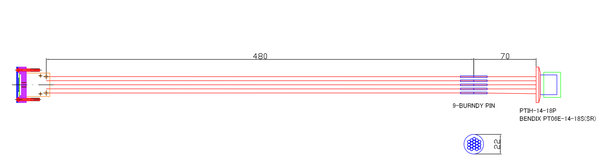
VIEW FROM DOWNSTREAM



L-HeII TARGET for E549/E570

2005/8/19 S. ISHIMOTO KEK





VIEW FROM UPSTREAM