SDD Back Plane Readout Test

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2005.8.15

Abstract

We tested the SDD back plane readout to get earlier signal timing. Taniguchi-san modified the power supply side circuit and made a discharge preamplifier. The back plane signal could be seen at room temperature, but the FET 2N4416 doesn't work correctly near 80 K, so local temperature control system was needed aside from SDDs. Moreover the circuit modification made the energy resolution bad, Mn Kα and Kβ X-rays couldn't be separated. Because time ran out, we gave up readout from the back plane and shifted our work to CAEN test.

1 Introduction

Previous SDD test experiment at E549 shows that SDD has about 3 μs time resolution. This makes Kaonic Helium X-rays S/N ratio lower, because more accidental π^- induced X-rays and gamma background from π^0 can be detected in a timing window of $K_{\rm stop}$. In order to realize good S/N ratio, an earlier signal timing is needed. That signal can be gotten from the SDD back plane which is a hole collection electrode (p^+ Si). The holes excited by X-rays drift to the back plane vertically, so the drift time is dependent on SDD thickness. Now our SDD thickness is 450 μm, horizontal radius is about 5 mm, and the hole mobility is about one-half as much as the electron one in Si, so the back plane signal timing can be 5 times earlier (see Figure 1).

2 Circuit Modification

We asked Taniguchi-san to modify power supply side circuit. The modified circuit is as Figure 2. To read out the back plane signal a FET 2N4416 is needed, so local temperature control for the FET is also needed. But it is difficult for our setup...

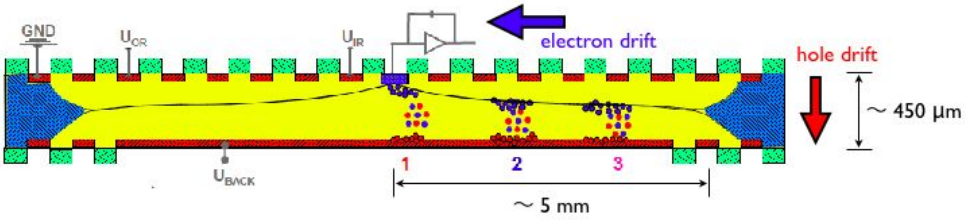


Figure 1: Electrons and holes drifting in SDD. Electrons drift horizontally up to 5 mm, on the other hand holes drift vertically up to 450 μm. In consideration of hole mobility (one-half of electron) the hole drift time is 5 times earlier than electron.

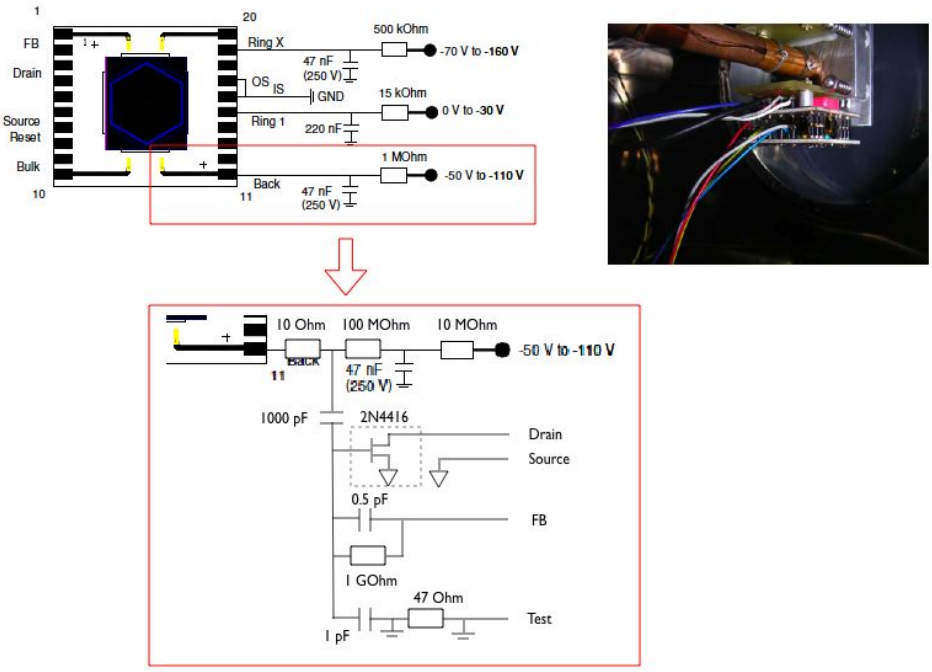


Figure 2: Modification of power supply side circuit by Taniguchi-san. The 1 GΩ resistance was replaced by 100 MΩ on our test because we couldn't get it in time from GND Co.

3 Test Results

3.1 Preamplifier Test

We tested a resistance discharge preamplifier made by Taniguchi-san. An FET 2N4416 and other elements were directly soldered on the preamplifier. For test pulse a NIM logic attenuated and widened was input to the preamplifier, that output is as Figure 3. The discharge time is about 100 μs, the rise time is about 100 ns (no figure).

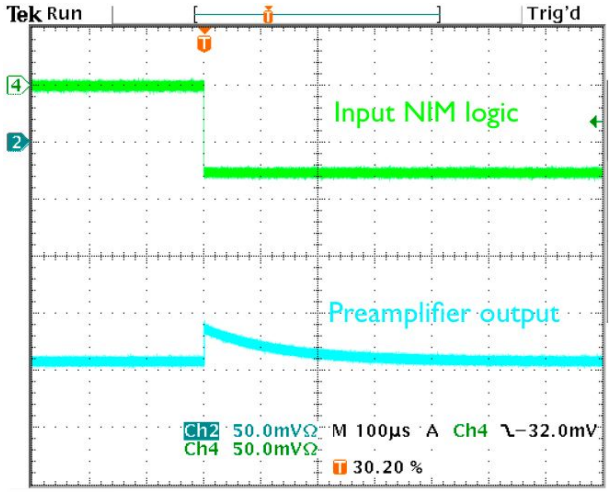


Figure 3: Discharge preamplifier test for back plane readout at room temperature. NIM logic was used for test pulse. Preamplifier discharge time is about 100 μs and the rise time is about 100 ns (no figure).

The shaping amp (ORTEC 570 shaping time 0.5 μs) output is as Figure 4. At room temperature the noise level is about $\pm$50 mV and S/N is about 5. So we can clearly discriminate the signal.

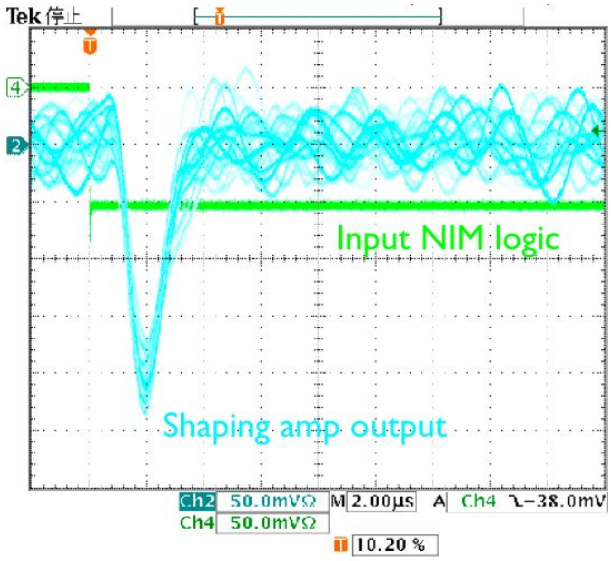


Figure 4: The shaping amp output at room temperature. Shaping amp is ORTEC 570, shaping time is 0.5 μs. At room temperature the noise level is about $\pm$50 mV and S/N is about 5.

3.2 SDD Circuit Test

Next we set the modified SDD circuit and tested. The test pulse was same NIM logic. The preamplifier output is as Figure 5. The signal was relatively small compared with previous preamplifier test.

Even so, SDD was set and radiated by ^{55}Fe source. The shaping amp output is as Figure 6. The noise level is same as previous test about $\pm$50 mV (included some offset), S/N is about 4.

At room temperature the signal was continuous, but at near 80 K the FET didn't work correctly, the signal output rate became about 1 Hz. Taniguchi-san said this may be caused by a slow relaxation oscillation. Actually several milliseconds oscillation was seen. We couldn't solve this problem.

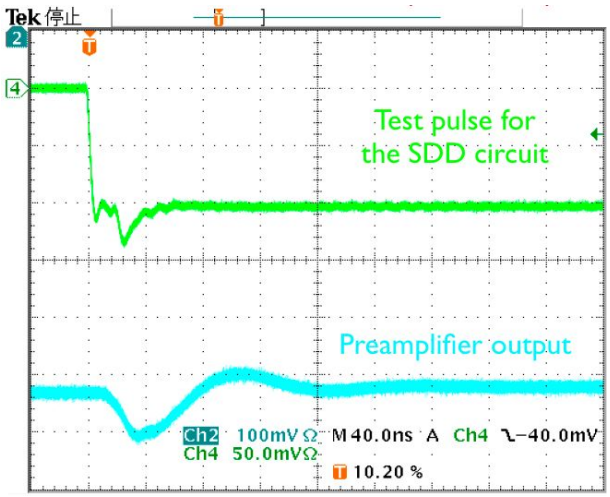


Figure 5: SDD circuit test at room temperature. The test pulse is same NIM logic. The preamplifier signal is relatively small compared with preamplifier only test.

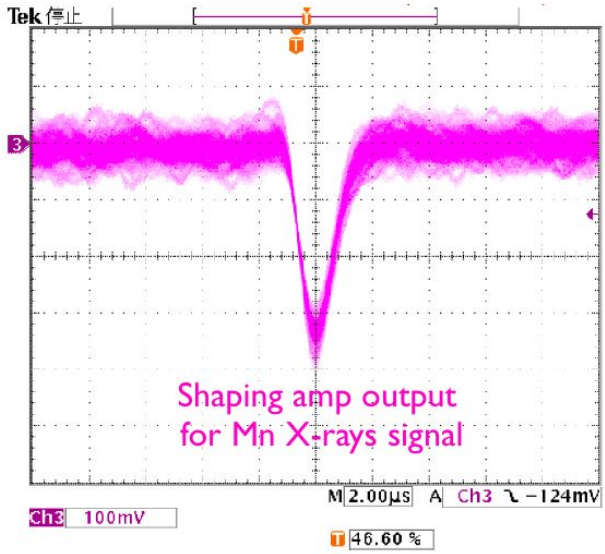


Figure 6: The shaping amp output for Mn X-rays at room temperature. The noise level is same as previous test about ±50 mV (included some offset), S/N is about 4.

3.3 Energy Resolution

We checked the SDD energy resolution on the condition of the modified circuit. Even if at 80 K, the resolution was very bad. The result is as Figure 7. Near 2500 ch peak is Mn K X-rays signal. Kα and Kβ couldn't be separated. The left side low channel peak is noise.

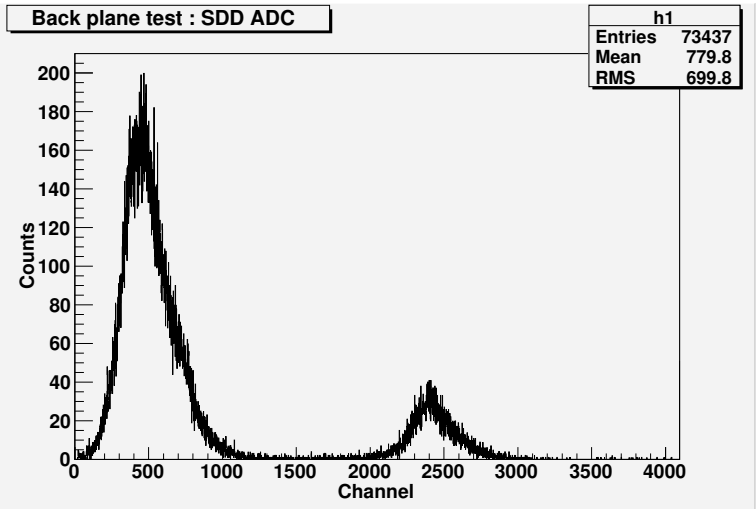


Figure 7: Energy spectrum at 80 K. Near 2500 ch peak is Mn K X-rays signal. Kα and Kβ couldn't be separated. The left side low channel peak is noise.

4 Conclusion

We tested the SDD back plane readout to get earlier signal timing. The back plane signal could be seen at room temperature, but the FET 2N4416 doesn't work correctly near 80 K. Moreover the circuit modification made the energy resolution bad, Mn Kα and Kβ X-rays couldn't be separated.

We couldn't solve these problems in time, so shifted our work to next dummy SDD test and CAEN module test.

E570 meeting

2005/08/15 S.Okada and H.Tatsuno

1 Test for a CAEN spectroscopy amplifier module "N568B"

We borrowed a CAEN 16 channel programmable spectroscopy amplifier "N568B" from SMI and also bought the same amplifier which will be delivered middle of September. Now we are checking the performance evaluations of borrowed N568B. Figure 1 shows front panel of N568B/LC, and Table 1 shows descriptions of outputs and inputs of N568B/LC.

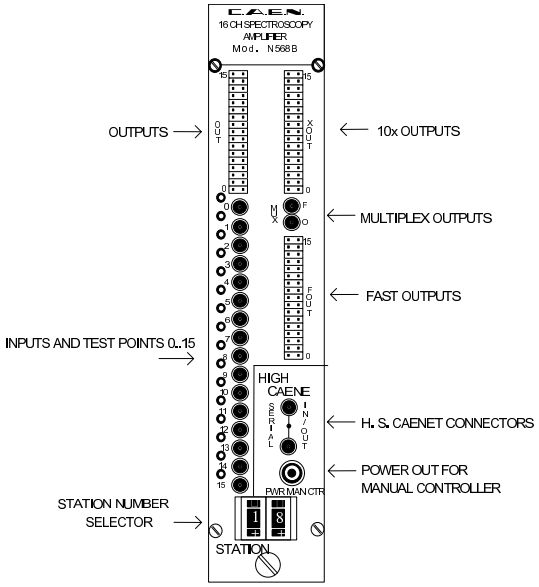


Figure 1: Mod. N568B/LC Front Panel

1.1 Output signals

Figure 2 shows output signals from CAEN N568B triggered by ORTEC 570 outputs of 0.5 μsec shaping time with reset veto. The fast output (MUX F) was very noisy. So we tried to reduce this noise using high-pass filters, however the noise could not be reduced sufficiently.

1.2 Delay time in the module

We found that the delay time in the module N568B is shorter than that of ORTEC 572 modules. Figure 3 shows the timing relation of signals from CAEN N568B and ORTEC 570. The CAEN N568B timing is 6 / 3 μsec faster than ORTEC 570 timing with 3 / 1 μsec shaping time.

Inputs	
INPUTS 0..15:	Positive or negative pulses with rise time $\geq$ 18 ns, max. amplitude: 8 V (absolute value); 50 Ω impedance. (1 kΩ impedance for Mod. N568BD)

Outputs	
OUT:	100 Ω impedance. Unipolar, dynamic range ±8 V max; polarity as selected in common with XOUT and MUXOUT.
XOUT:	100 Ω impedance. Unipolar, further 10x fixed amplification of the OUT value, dynamic range ±4 V max into 100 Ω load; polarity as selected in common with OUT and MUXOUT.
FOUT:	100 Ω impedance. Unipolar, 100 ns Differentiation Time Constant, ±4 V max into 100 Ω load. Risetime: 25 ns typically. Gain factor: 7 to 10 for non inverting configuration, 20 to 30 (approx.) for inverting configuration.
MUX O:	100 Ω impedance. Unipolar, ±8 V max; polarity as selected in common with OUT. Selected channel is the last accessed via H.S. CAENET. Can be disabled via CAENET.
MUX F:	100 Ω impedance. Unipolar, amplitude 85% approx. of FOUT amplitude. Selected channel is the last accessed via H.S. CAENET. Can be disabled via CAENET.

Table 1: Inputs and outputs of Mod. N568B/LC

1.3 Reset signal timing

The reset timing of N568B is therefore faster than that of ORTEC 570/572 modules and reset pulse signal which is directory got out from the reset pulse in the preamp. Figure 4 shows the timing relation of reset pulse signal timings: fast output of CAEN module (MUX F), normal output of CAEN module (MUX O) with 0.2μsec shaping time, ORTEC 570 output with 0.5μsec shaping time and reset pulse output got out from the preamp. Thus we cannot use the reset pulse signal got out from the preamp for reset veto, because the output signal from N568B is too fast.

Though fast output of CAEN module cannot use for timing signal information due to large noise, the output may be used for reset pulse signal to make the reset veto gate.

1.4 Input impedance probrem

We found that the input impedance of borrowed CAEN module is not 1 kΩ. If the model name of this moudle is "N568BD", the input impedance must be 1 kΩ. We need to confirm if it is really "N568BD" or not.

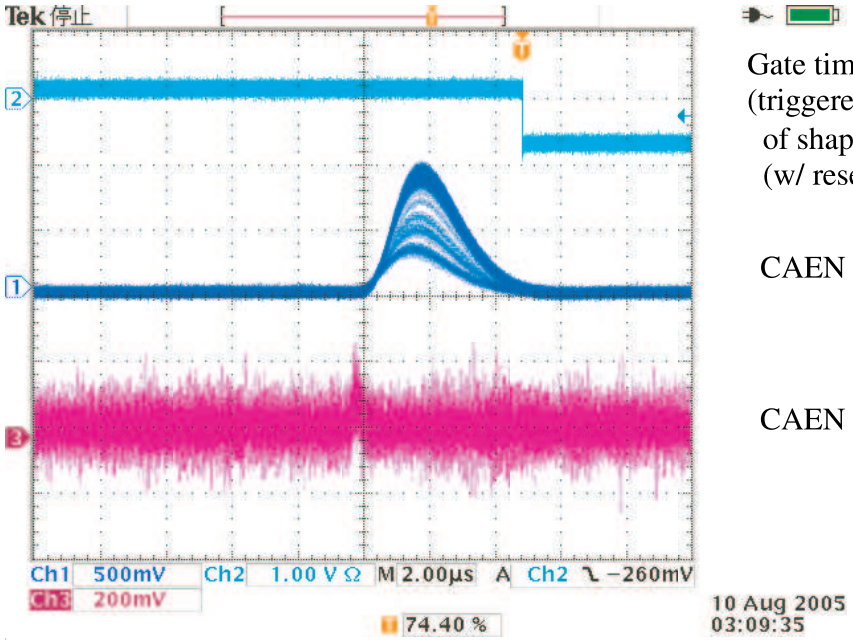
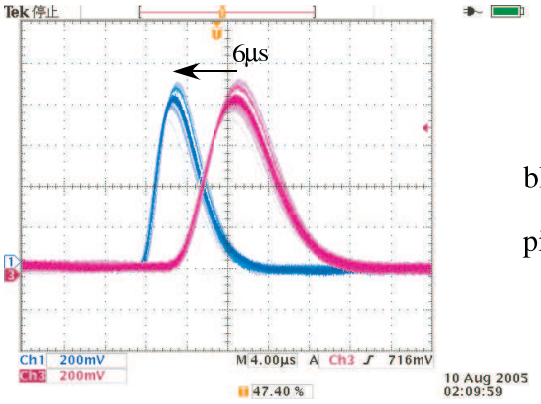


Figure 2: Outputs of CAEN module

Shaping time : 3µs



blue : CAEN MUX O

pink : ORTEC572

Shaping time : 1µs

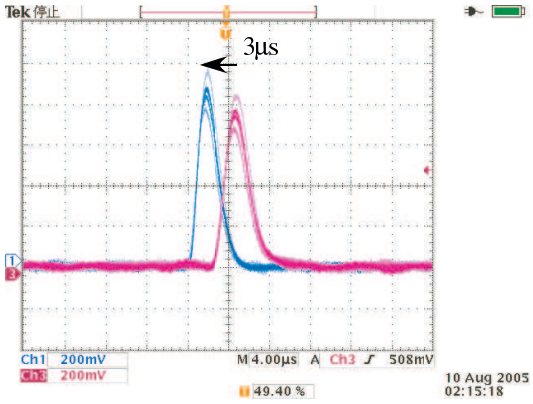


Figure 3: Timing relation of signals from CAEN N568B and ORTEC 570

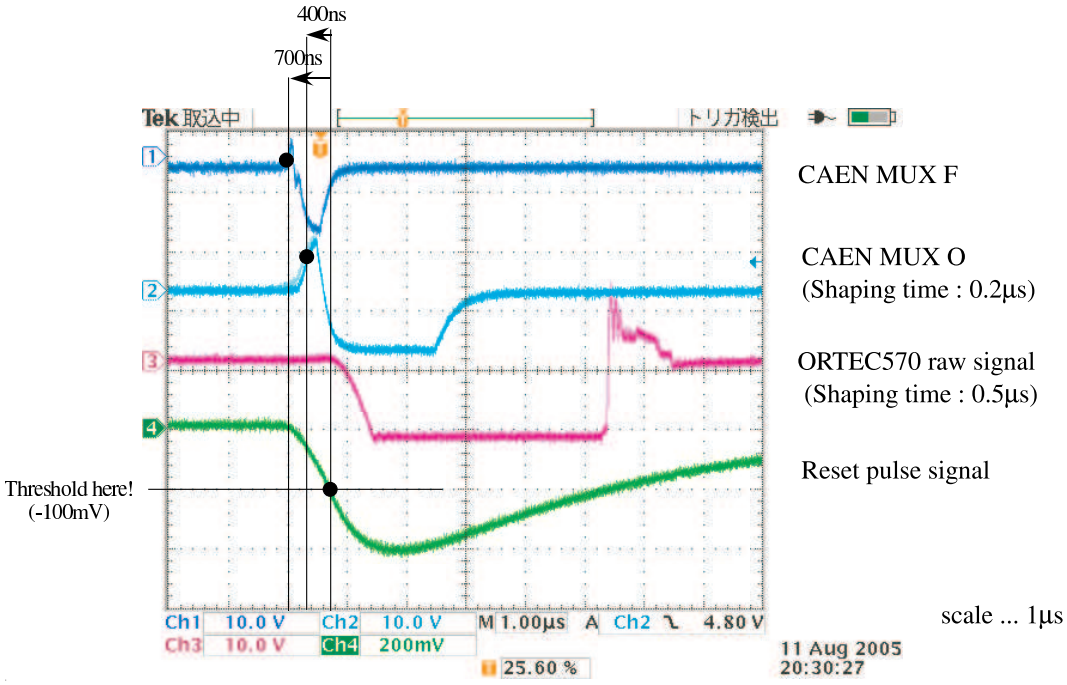


Figure 4: Timing relation of reset pulse signals

2 Preparation status of E570

2.1 SDD

2.1.1 SDD

- New two SDDs and four preamps were delivered to RAL. Matsuzaki-san (or Ishida-san) will bring them from RAL to RIKEN on 15th Aug.
- The repair on the 100 mm^2 SDD "V2-8-05.04" was finished by KETEK. They said that they made a goodwill repair and do not charge the costs of repair. We just have to bear the costs for the delivery.
  → Matsuda-san will bring it from RAL to RIKEN on 22th Aug.

2.1.2 Preamp

Preamp box and its support were designed and ordered to CI company. They will be delivered at 23th Aug.

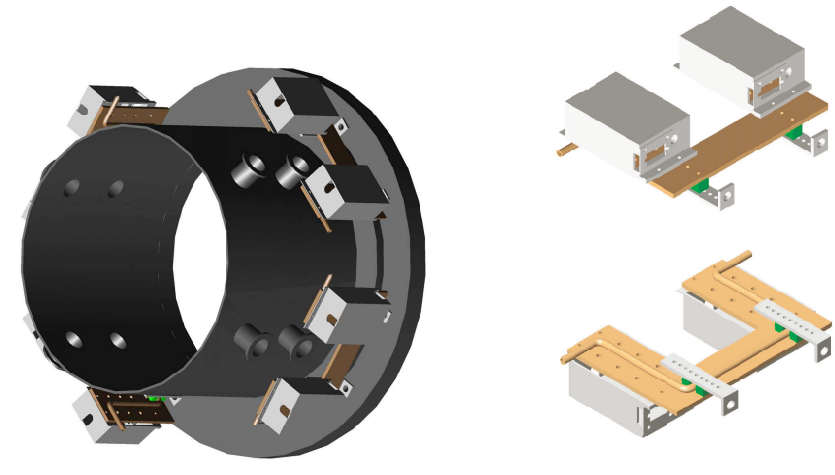


Figure 5: Preamp box and its support

2.1.3 SDD support

Aluminum holders for SDDs were ordered to CI company and will be delivered 23th Aug.

2.2 Electronics

2.2.1 TDC

TKO TDCs (HR-TDC) modified to have long full range (1μsec→5μsec) by REPIC will be delivered within this week. (cost : 28,455JPY)

2.2.2 Conversion board

The output connector for CAEN spectroscopy amplifier is 17+17 pin double row strip header type (left pin:ground, right pin:signal), which can be connected to 34 pin flat cable connector. The connector for FOUT (FAST OUTPUTS) should be converted to lemo type, since the FOUT signals are required for trigger scheme and thus should be discriminated. We have conversion boards of 40 pin flat cable connector into 16 channel lemo connectors in KEK electronics equipment pool. When we use the conversion boards, we need to use a conversion cable of 40 pin flat cable connector to 34 pin's one. In order to reduce the noise source due to the connection of the flat cable, we ordered the conversion boards of 34 pin flat cable connector directory into 16 channel lemo connectors. It will be delivered end of this month (by REPIC).
(cost : 57,225JPY(initial cost) + 6,700JPY(per one board)(when we supply lemo connectors))

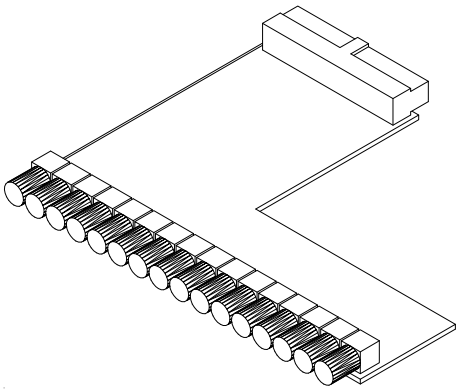


Figure 6: Conversion board of 34 pin flat cable connector into 16 channel lemo connectors (see Figure 1 (Mod. N568B/LC Front Panel))

2.3 Foils

2.3.1 Pure Ni and Ti

Ni sheets (100×100×0.05 ×2sheets) were already delivered from GoodFellow company.
Ti sheets (100×100×0.125 ×4sheets) will be delivered middle of Aug.

2.3.2 Pure Al

Al sheets (100×300×0.3 ×15sheets) were already delivered from Nirako company.

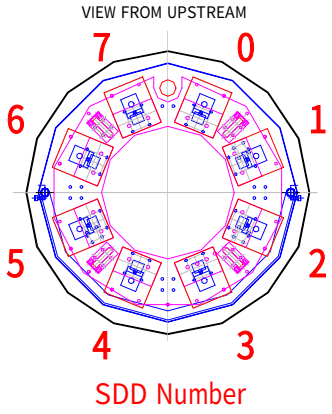
Progress report of the LHeII Target for E570 experiment

Shigeru Ishimoto, Masami Iio

・The LHeII target is being modified to set SDD's in the liquid N_2 radiation shield.

<The items, which finished work by Aug 13th.>

(1) Calibration of 8 Pt100-thermometers in L-N2 and 300K



Sensor : Rt100 (CLASS A),
Current : **1 mA** (ADVANTEST R6144 voltage/current Generator)
Vol. readout : ADVANTEST R6552 Digital Multimeter

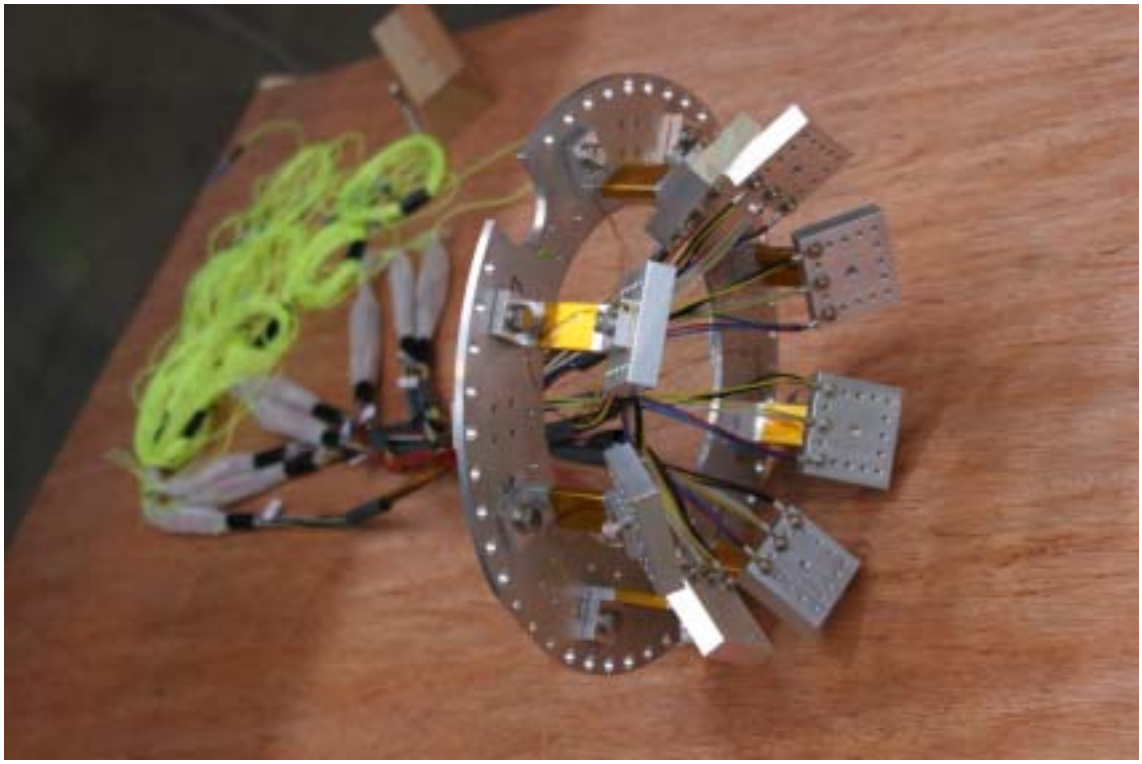
SDD No.	Pt100 Serial No.	Room Temp (mV)	LN2 Temp (mV)	LN2 Temp (K)
0	1484	109.77	20.72	77.60
1	1485	109.62	20.78	77.74
2	1486	109.94	20.74	77.65
3	1487	109.76	20.53	77.13
4	1489	109.75	20.54	77.15
5	1491	109.56	20.68	77.50
6	1495	109.65	20.52	77.11
7	1498	109.70	20.74	77.65

➔ Pt100-thermometers were not wrong about 1K

(2) Fabrication of the 8 vacuum connectors and cables for 8 Pt100-thermometers and 4 heaters from 8 vacuum connectors to the datalogger /LakeShore-340

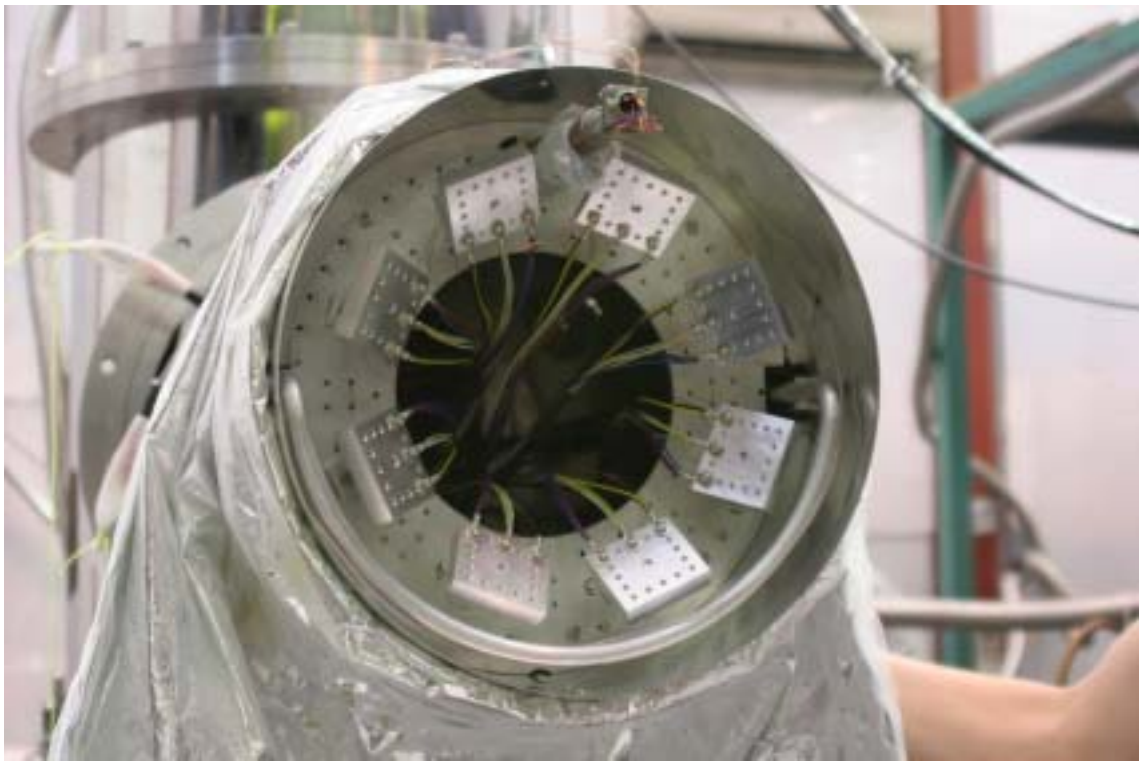
・**A cable is identified in the combination of a 4 colors and the 3 colors of shrink tube.**
The color of shrink tube is Red or White ➔ SDD's cable
The color of shrink tube is Black ➔ Thermometer's cable or heater's cable
(Only the 7th port has two cables of a heater.)

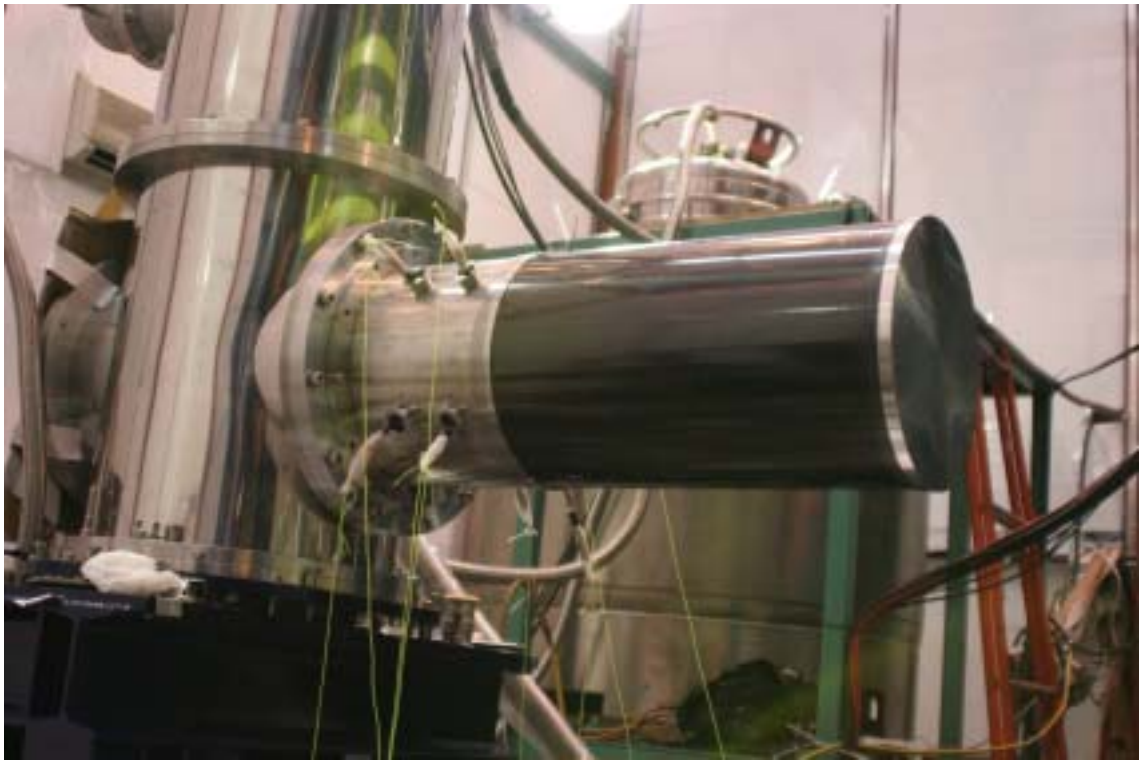
(3) Set up SDD support parts with 8 dummy SDD's, including 8 Pt100-thermometers, 4 heaters and cables from SDD's to vacuum connectors



(4) Fabrication and assemble of CFRP vacuum pipe and 8 18pin-connectors

(5) Assemble test of cryogenic parts





Some photos of these assemble parts and setting process were taken and uploaded at next URL.

http://ishimotopc2.kek.jp/LHeIIT/050813/E570-01.html

<The tasks, which will be planned from Aug 15th>

(a) Re-assemble SDD support parts with the L-HeII target cell (backup)
(b) Wiring to Keithley 2700 (data logger) and Lake Shore 340 (controller) ← We need to help of Sato-san?
(c) Leak test of new CFRP vacuum pipe at room temperature
(d) L-N2 cooling --> Temperature and heater control test
(e) L-He cooling --> Measurement of L-He consumption from 1K parts